ECE 4401 Fall 2014
Digital Design Laboratory

Th 2:00-2:50pm Gent 203, 3:00-6:00pm ITEB C30

***Course Description**: Three Credits. Prerequisite: ECE 3401.* Digital designing with PLA and FPGA, A/D and D/A conversion, floating point processing, ALU design, synchronous and asynchronous controllers, control path; bus master; bus slave; memory interface; I/O interface, logic circuits analysis, testing, and trouble shooting; PCB; design and manufacturing.

Instructor: Omer Khan
Office: ITEB 439 Tel.: (860) 486-2192
Email: khan@uconn.edu
Office Hours: by appointment via email
Website: http://www.engr.uconn.edu/~omer.khan/courses/ece4401_f14/index.html

TA: Farrukh Hijaz
Office: ITEB 314
Email: farrukh.hijaz@uconn.edu
Office Hours: by appointment via email

Optional Text: ***The Student's Guide to VHDL***, Peter J. Ashenden

Lab Hours: M-F 9-5 (except when other classes are being held – ECE3411 M 2:30-6:30pm; ECE2001W Tu 9am-9pm, Th 11-1pm; ECE3201 W 10:10am-12:10pm, 2:30-4:30pm). If lab is locked contact someone in the ECE main office in ITEB 4th floor.

Grading Policy:	Quiz and Class Participation	10%
	Labs	70%
	Final Project	20%

Tentative Schedule:

Lecture	Date	Thursday	Deliverable (**Hard Deadlines***)
1	08/28	Lab 1: Introduction, 7-segment-LED Display	
2	09/04	Lab 2: Calculator Design	
3	09/11	Lab 3: Vending Machine (FSM Design)	Lab 1+2
4	09/18	Lab 4: Getting Started with Bus Interface	Lab 3
5	09/25	Lab 5: PS/2 Keyboard Interface	Lab 4
6	10/02	Lab 6: Memory Access Controller: SRAM I/F	Lab 5
7	10/09	Lab 7: Keyboard/SRAM LED Display Lab 8: VGA Interface & Text VGA Display	Lab 6
8	10/16	Lab 9: Microcontroller I/F and VGA Display	Lab 7
9	10/23	Makeup lecture	Lab 8
10	10/30	**In-class Quiz**; D/A and PWM	Lab 9
11	11/06	Final Project	Project outline**
12	11/13	Final Project	
13	11/20	Final Project	Project mid-review
14	12/04	Final Project	Project presentation/Demo

* Labs will be due in class (or earlier via email). A late penalty of 50% reduction in total for the lab will be applied after the deadline. Lab grade of 0 will be applied if >1 week late.

** Proposal must include specification, interfaces, a block diagram, and deliverables for your proposed design.