AMI C5N Process Design Rules

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Note:

Most of the contents in this document were taken from the MOSIS website http://www.mosis.org/

MOSIS Layer Map for AMI_C5N

This is the layer map for the AMI C5N 0.5 micron 3 metal, 2 poly (non-silicided) layout rules (AMI_C5N), and only for those AMI vendor design rules. For designs that are laid out using other design rules (or technology-codes), use the standard layer mapping conventions of that design rule set.

Layer	GDS	CIF	Notes
N_WELL	1	A01	
ACTIVE	2	A02	
N_CHANNEL_FLD	3	A03	Optional; if omitted a copy of the drawn N_WELL is used.
POLY	4	A04	
N_PLUS_BLOCK	5	A05	AMI calls this layer N_PLUS_SELECT and further requires that it be a copy of P_PLUS_SELECT. It is functionally an N_PLUS_BLOCK layer; the drawn regions will _not_ receive the n+ implant.
P_PLUS_SELECT	6	A06	
CONTACT	8	A08	
METAL1	9	A09	
VIA1	10	A10	
METAL2	11	A11	
VIA2	12	A12	
METAL3	13	A13	
CAP_POLY (POLY2)	26	A26	Optional
HRP (HIGH RESISTANCE)	27	A27	
GLASS	14	A14	

Fig. 1. AMI original layer mapping.

If you use MOSIS SCMOS design rules, you should use the layer map for technology codes SCN3ME and SCN3ME_SUBM, and only for SCN3ME and SCN3ME_SUBM. For designs that are laid out using other design rules (or technology-codes), use the standard layer mapping conventions of that design rule set.

SCN3ME: Scalable CMOS N-well, 3 metal, non-silicided, high resistance layer available. Adds a second polysilicon layer (poly2) as the upper electrode of a poly capacitor.

SCN3ME_SUBM: Uses revised layout rules for better fit to sub-micron processes (see MOSIS Scalable CMOS (SCMOS) Design Rules, section 2.4).

Layer	GDS	CIF	CIF Synonym	Rule Section	Notes
N_WELL	42	CWN		1	
ACTIVE	43	CAA		2	
POLY	46	CPG		3	
N_PLUS_SELECT	45	CSN		4	
P_PLUS_SELECT	44	CSP		4	
POLY2	56	CP2	CEL	11, 12, 13	Optional
HI_RES_IMPLANT	34	CHR		27	Optional
CONTACT	25	CCC	CCG	5, 6, 13	
POLY_CONTACT	47	CCP		5	Can be replaced by CONTACT
ACTIVE_CONTACT	48	CCA		6	Can be replaced by CONTACT
POLY2_CONTACT	55	CCE		13	Can be replaced by CONTACT.
METAL1	49	CM1	CMF	7	
VIA	50	CV1	CVA	8	
METAL2	51	CM2	CMS	9	
VIA2	61	CV2	CVS	14	
METAL3	62	CM3	CMT	15	
GLASS	52	COG		10	
PADS	26	XP			Non-fab layer used to highlight pads
Comments	--	CX			Comments

Fig. 2. Fabricated on AMI 0.50 micron process runs.

This is the layer map for the whole MOSIS Scalable CMOS layout rules.

Layer	GDS	CIF	CIF Synonym	Rule Section	Notes
N_WELL	42	CWN		1	SCN* and SCE*
P_WELL	41	CWP		1	SCP* and SCE*
CAP_WELL	59	CWC		17, 18	SC*LC
ACTIVE	43	CAA		2	
THICK_ACTIVE	60	CTA		24	TSMC 0.25 µ, TSMC 0.35 µ SC*
PBASE	58	CBA		16	SC*A
POLY_CAP1	28	CPC		23	SC*PC
POLY	46	CPG		3	
SILICIDE_BLOCK	29	CSB		20	HP 0.5 µ SC*, TSMC 0.25 µ SC*, TSMC 0.35 µ SC*1P*
N_PLUS_SELECT	45	CSN		4	
P_PLUS_SELECT	44	CSP		4	
ELECTRODE	56	CEL		11, 12, 13	
HI_RES_IMPLANT	34	CHR		27	AMI 0.5 µ SC* designs only
CONTACT	25	CCC	CCG	5, 6, 13	
POLY_CONTACT	47	CCP		5	Can be replaced by CONTACT
ACTIVE_CONTACT	48	CCA		6	Can be replaced by CONTACT
ELECTRODE_CONTACT	55	CCE		13	SC*E, SC*A Can be replaced by CONTACT.
METAL1	49	CM1	CMF	7	
VIA	50	CV1	CVA	8	
METAL2	51	CM2	CMS	9	
VIA2	61	CV2	CVS	14	SC*3M
METAL3	62	CM3	CMT	15	SC*3M
VIA3	30	CV3	CVT	15, 21	SC*4M
METAL4	31	CM4	CMQ	22	SC*4M
CAP_TOP_METAL	35	CTM		28	TSMC 0.25 µ SC*
VIA4	32	CV4	CVQ	25	SC*5M
METAL5	33	CM5	CMP	26	SC*5M
VIA5	36	CV5		29	
METAL6	37	CM6		30	
GLASS	52	COG		10	
PADS	26	XP			Non-fab layer used to highlight pads
Comments	--	CX			Comments

The following figure is a cross-section view of some popular components fabricated with AMI C5N technology. Here the resistor is fabricated with high-resistor and electrode (poly2) layers, and capacitor with poly1-poly2 layers.

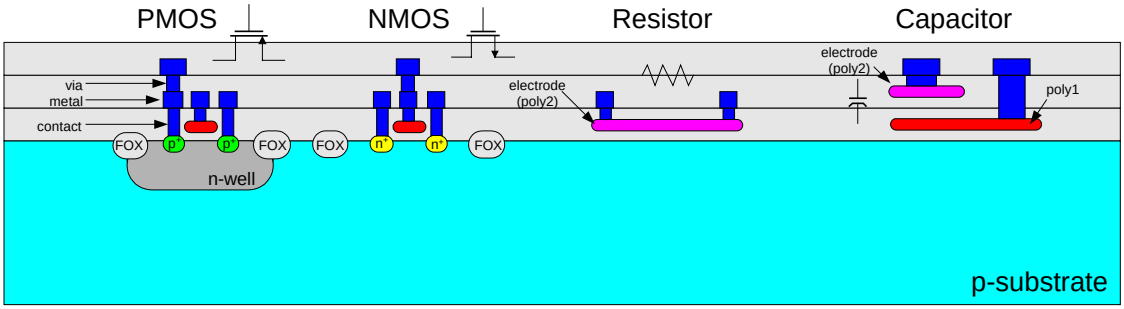
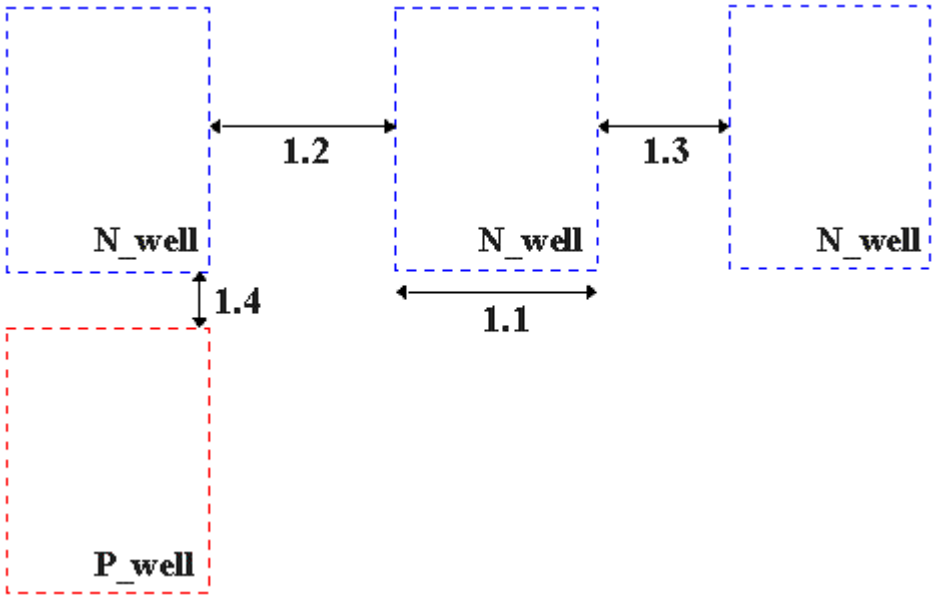


Fig. 4. Some popular used components fabricated with AMI C5N technology.

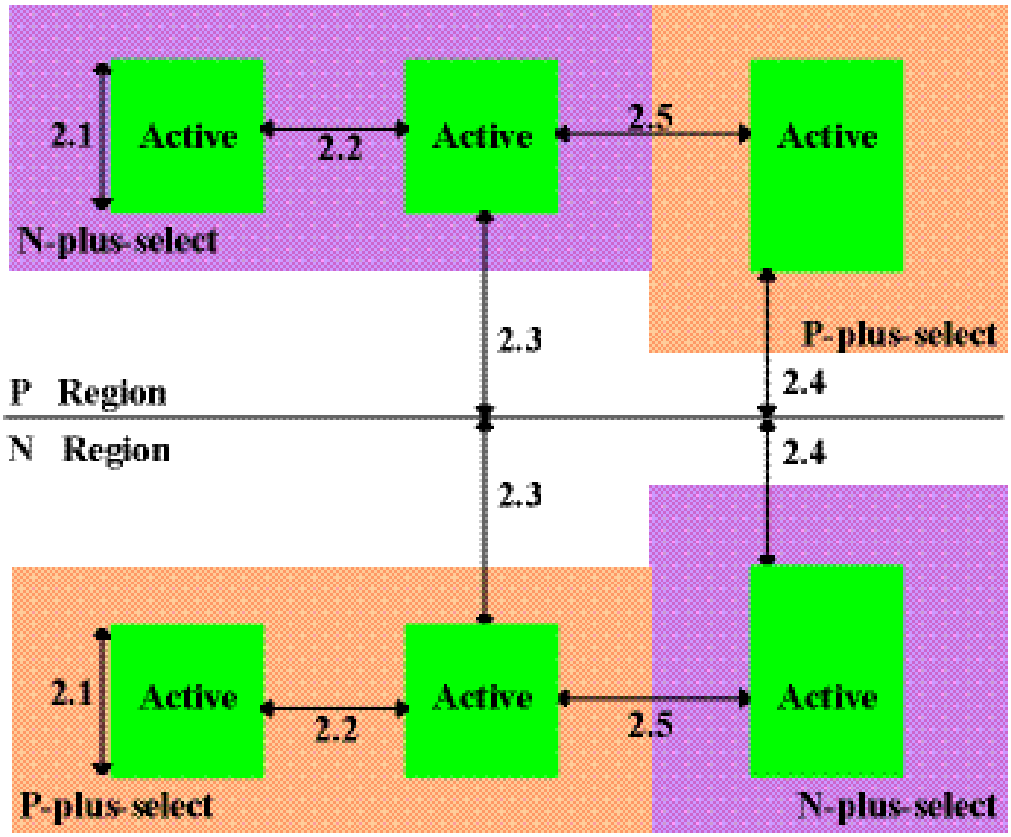
SCMOS Layout Rules - Well

Rule	Description	Lambda
1.1	Minimum width	10 [SUBM 12]
1.2	Minimum spacing between wells at different potential	9 [SUBM 18]
1.3	Minimum spacing between wells at same potential	0 or 6
1.4	Minimum spacing between wells of different type (if both are drawn)	0



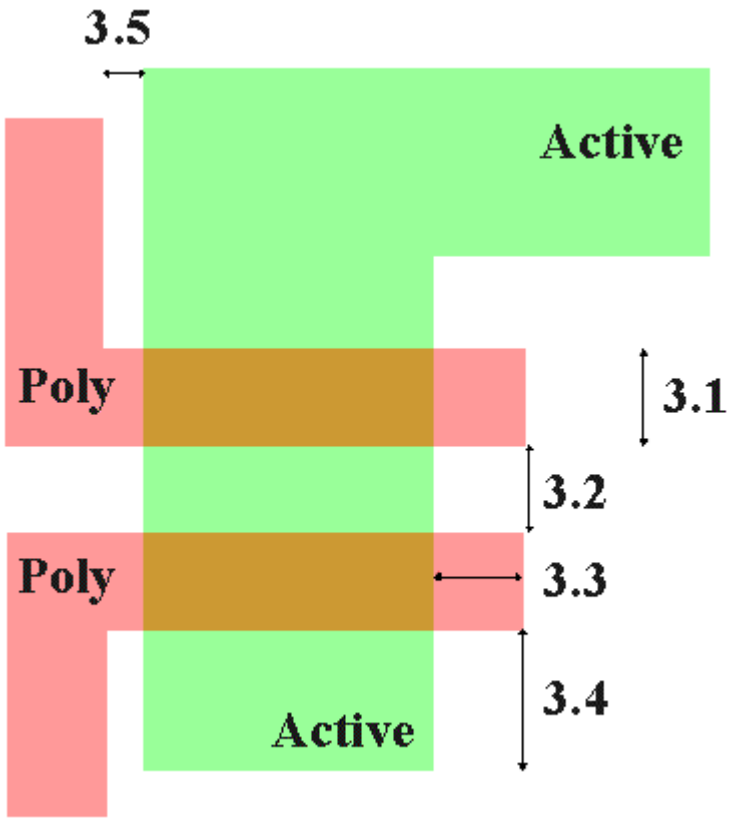
SCMOS Layout Rules - Active

Rule	Description	Lambda
2.1	Minimum width	3
2.2	Minimum spacing	3
2.3	Source/drain active to well edge	5 [SUBM 6]
2.4	Substrate/well contact active to well edge	3
2.5	Minimum spacing between active of different implant	0 or 4



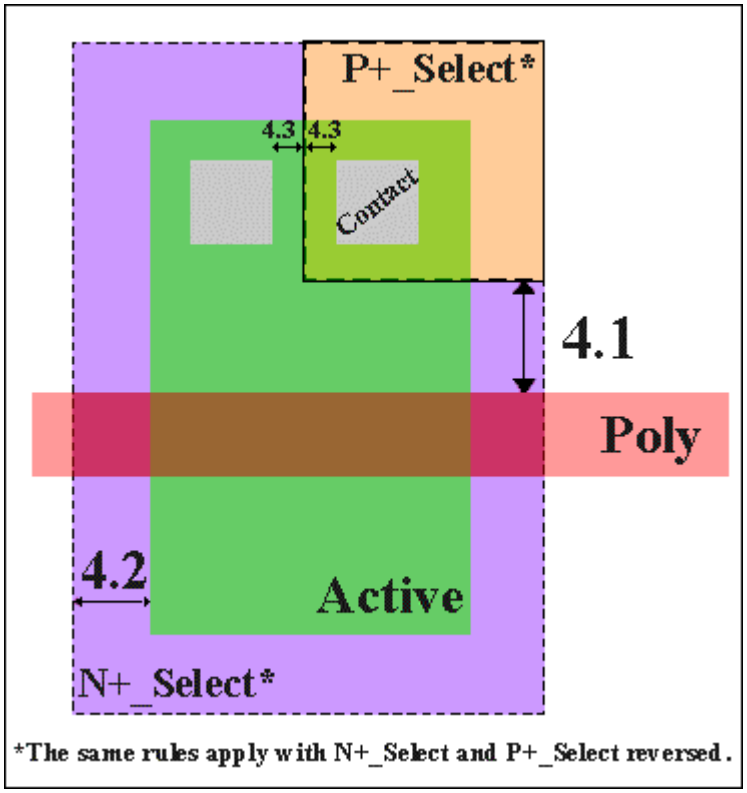
SCMOS Layout Rules - Poly

Rule	Description	Lambda
3.1	Minimum width	2
3.2	Minimum spacing over field	2 [SUBM 3]
3.2.a	Minimum spacing over active	2 [SUBM 3] [DEEP 4]
3.3	Minimum gate extension of active	2 [DEEP 2.5]
3.4	Minimum active extension of poly	3
3.5	Minimum field poly to active	1



SCMOS Layout Rules - Select

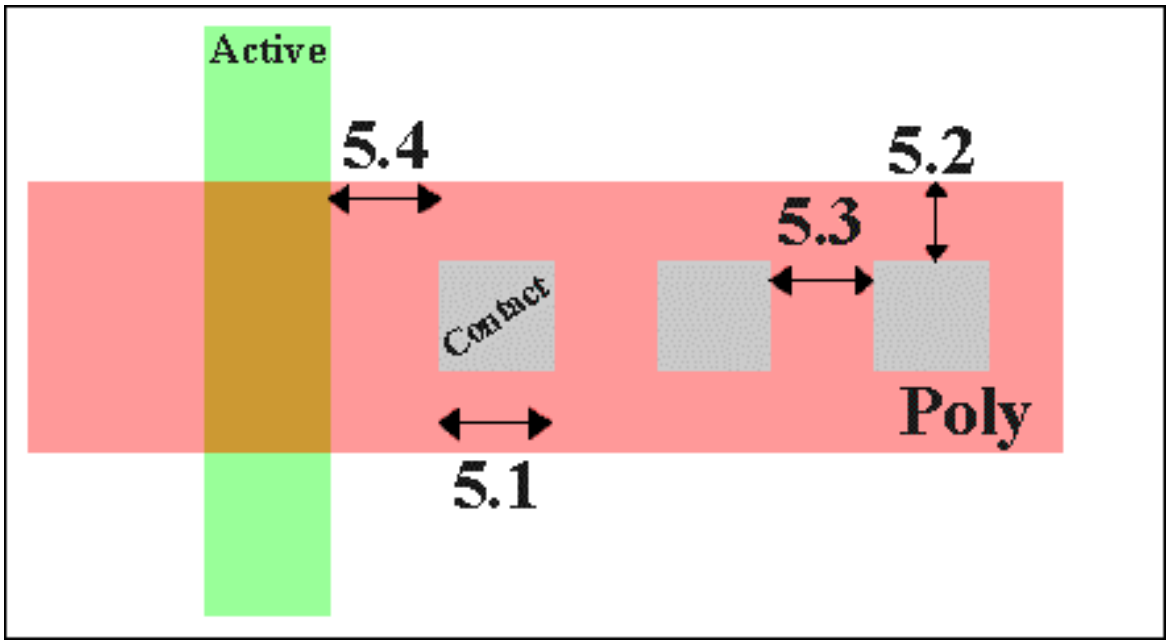
Rule	Description	Lambda
4.1	Minimum select spacing to channel of transistor to ensure adequate source/drain width	3
4.2	Minimum select overlap of active	2
4.3	Minimum select overlap of contact	1
4.4	Minimum select width and spacing (Note: P-select and N-select may be coincident, but must *not* overlap) (not illustrated)	2 [DEEP 4]



SCMOS Layout Rules - Simple Contact to Poly

On 0.5um process (and all finer feature size processes), it is required that ALL features on the insulator layers (CONTACT, VIA, VIA2) MUST BE of the single standard size; there are no exceptions for pads (or logos, or anything else); large openings must be replaced by an array of standard sized openings.

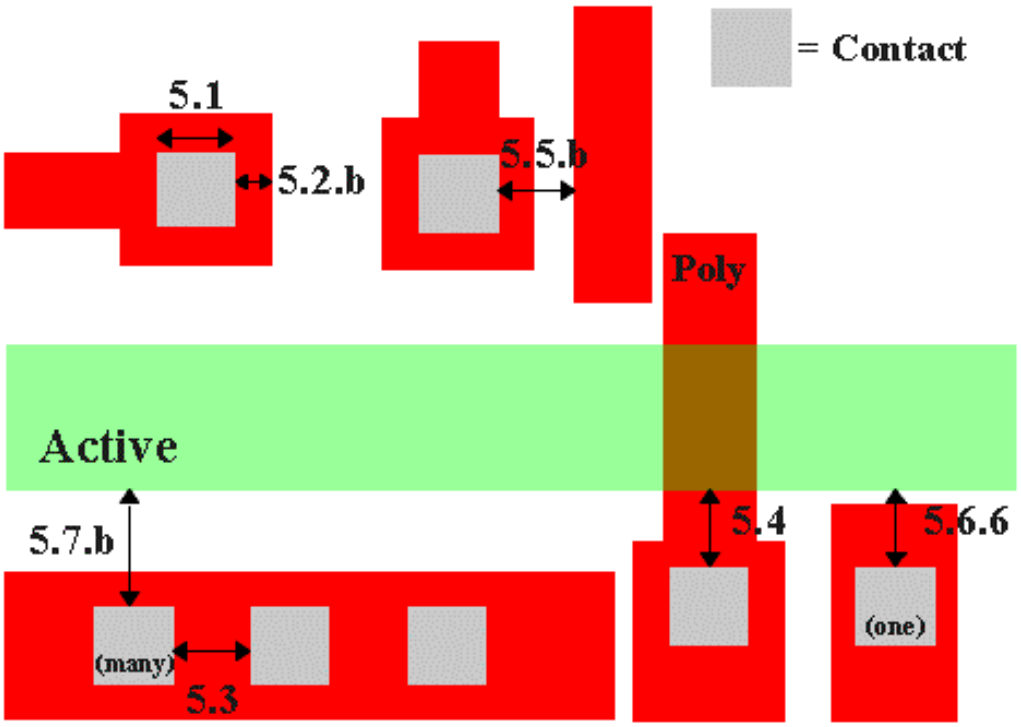
Rule	Description	Lambda
5.1	Exact contact size	2 x 2
5.2	Minimum poly overlap	1.5
5.3	Minimum contact spacing	2 [SUBM 3] [DEEP 4]
5.4	Minimum spacing to gate of transistor	2



SCMOS Layout Rules - Alternative Contact to Poly

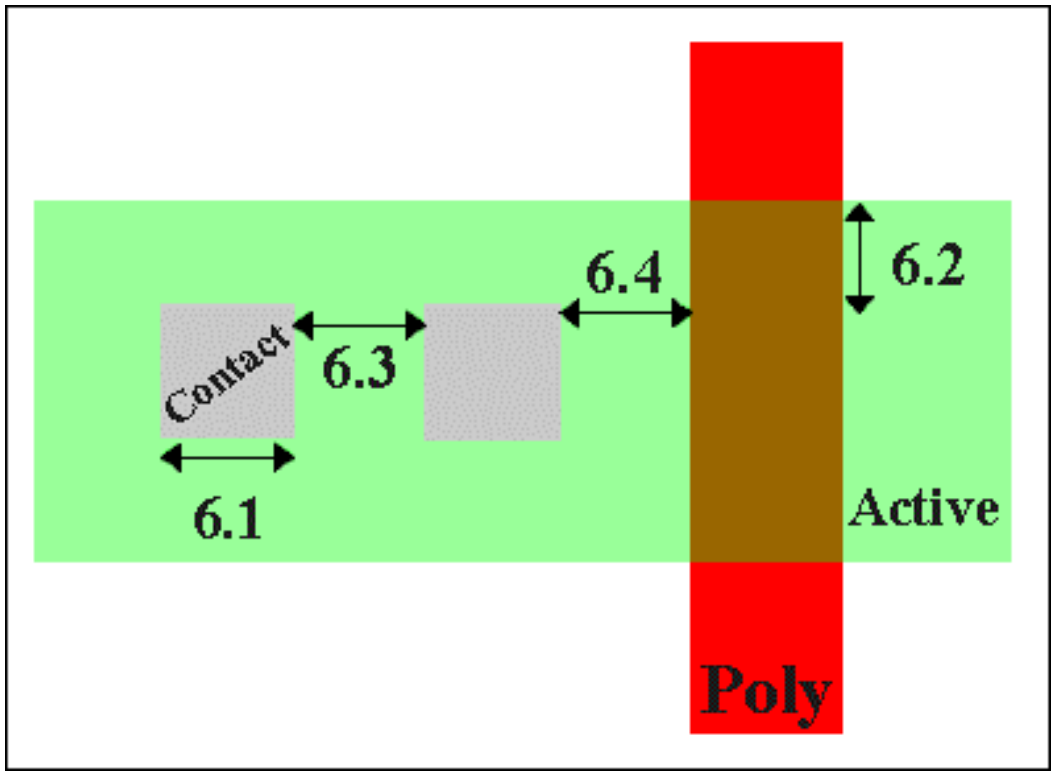
The rules above are preferred. If, however, one cannot handle the 1.5 lambda contact overlap in 5.2, then that rule, 5.2, may be replaced by these rules, which reduce the overlap, but increase the spacing to surrounding features. The remaining rules above, 5.1, 5.3, and 5.4, still apply as originally stated.

Rule	Description	Lambda
5.2.b	Minimum poly overlap	1
5.5.b	Minimum spacing to other poly	4 [SUBM 5]
5.6.b	Minimum spacing to active (one contact)	2
5.7.b	Minimum spacing to active (many contacts)	3



SCMOS Layout Rules - Simple Contact to Active

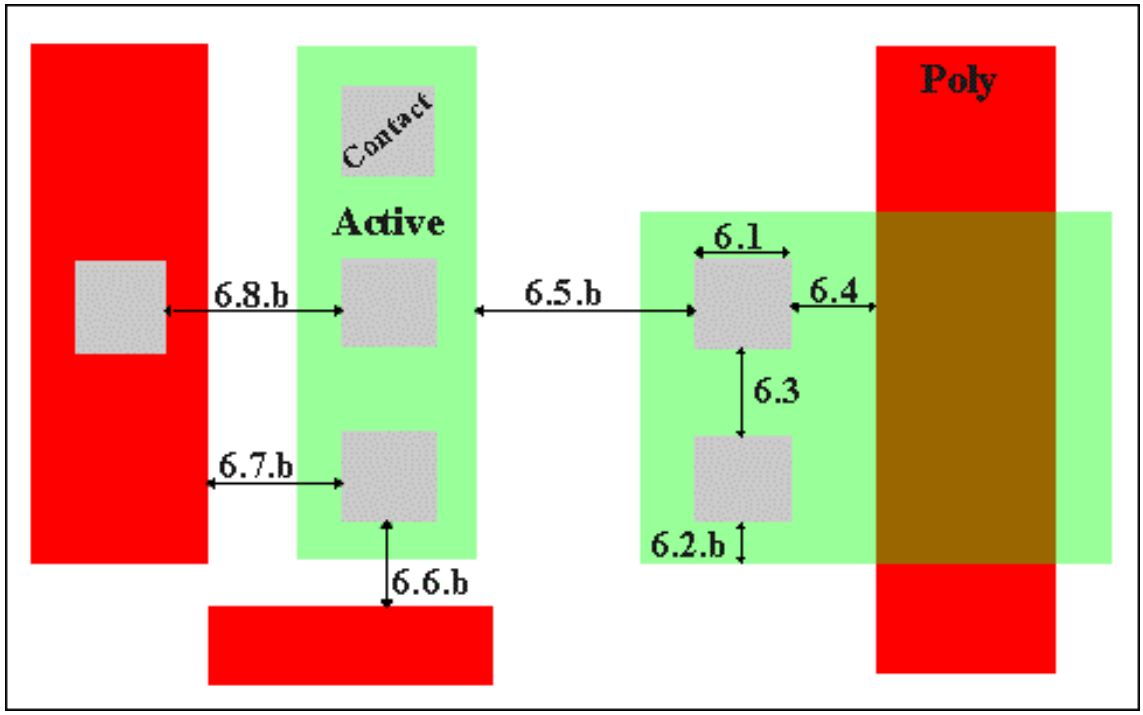
Rule	Description	Lambda
6.1	Exact contact size	2 x 2
6.2	Minimum active overlap	1.5
6.3	Minimum contact spacing	2 [SUBM 3] [DEEP 4]
6.4	Minimum spacing to gate of transistor	2



SCMOS Layout Rules - Alternative Contact to Active

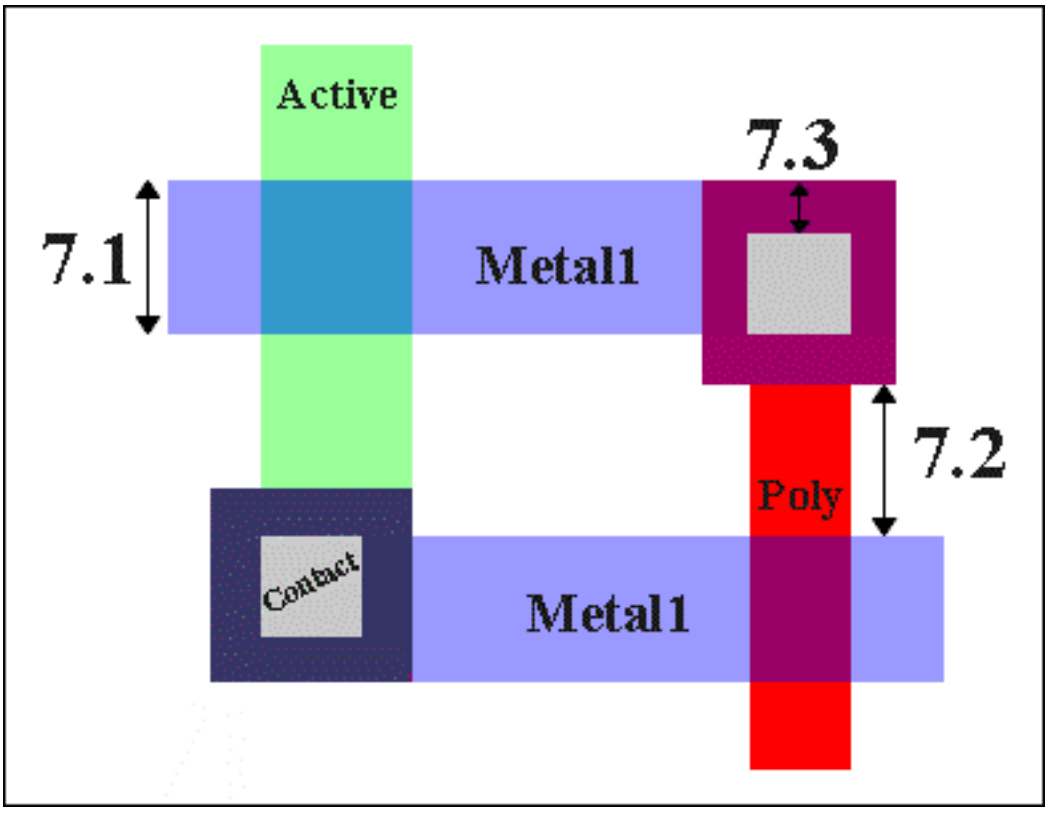
The rules above are preferred. If, however, one cannot handle the 1.5 lambda contact overlap in 6.2, then that rule, 6.2, may be replaced by these rules, which reduce the overlap, but increase the spacing to surrounding features. The remaining rules above, 6.1, 6.3, and 6.4, still apply as originally stated.

Rule	Description	Lambda
6.2.b	Minimum active overlap	1
6.5.b	Minimum spacing to diffusion active	5
6.6.b	Minimum spacing to field poly (one contact)	2
6.7.b	Minimum spacing to field poly (many contacts)	3
6.8.b	Minimum spacing to poly contact	4



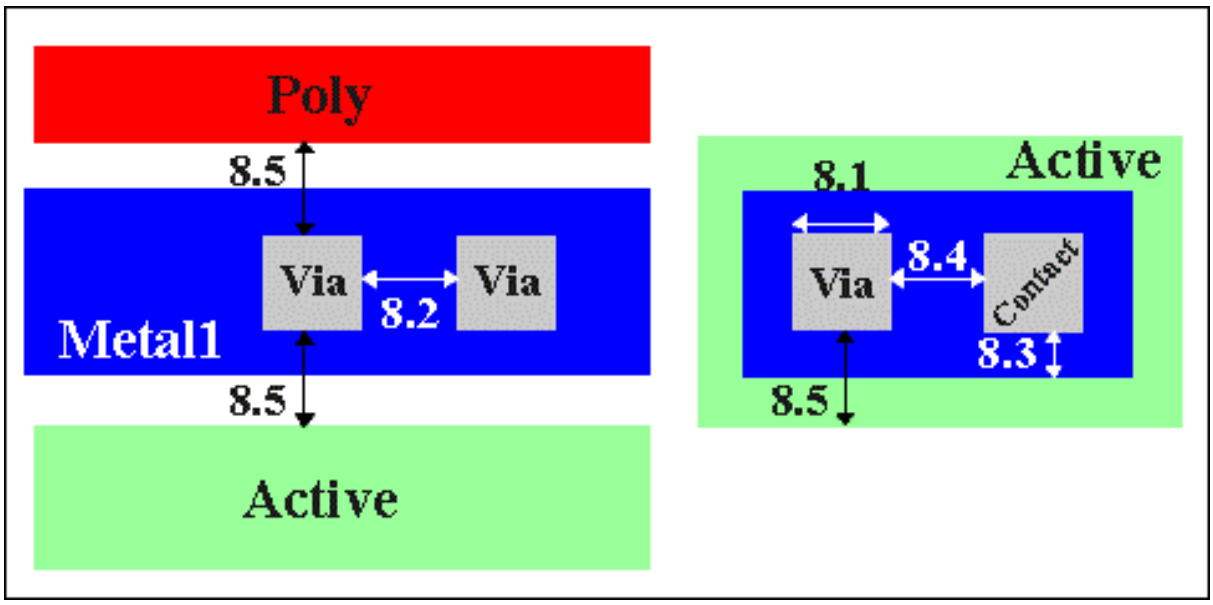
SCMOS Layout Rules - Metal1

Rule	Description	Lambda
7.1	Minimum width	3
7.2.a	Minimum spacing	3
7.2.b	Minimum tight metal spacing *(only allowed between minimum width wires - otherwise, use regular spacing rule)*	2
7.3	Minimum overlap of any contact	1



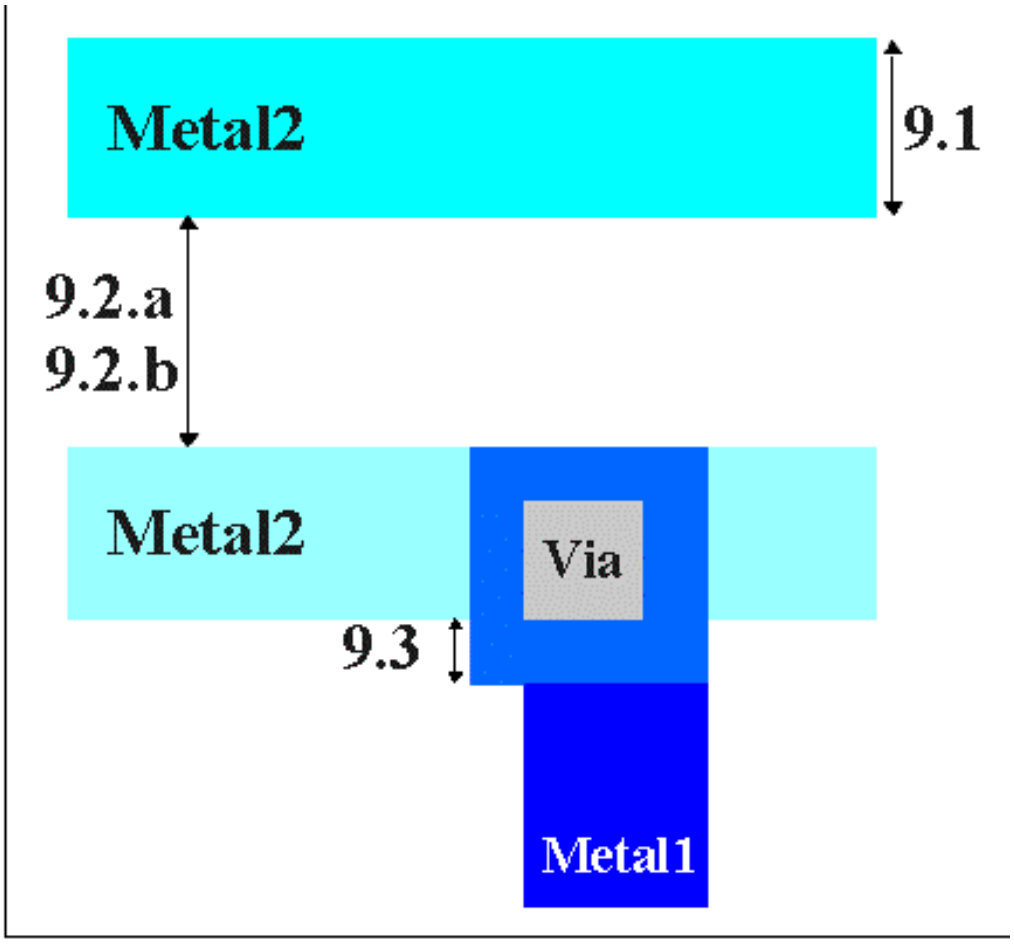
SCMOS Layout Rules - Via1

Rule	Description	Lambda
8.1	Exact size	2 x 2
8.2	Minimum via1 spacing	3
8.3	Minimum overlap by metal1	1
8.4	Minimum spacing to contact	2
8.5	Minimum spacing to poly or active edge (SCMOS only, not SUBM, DEEP)	2



SCMOS Layout Rules - Metal2

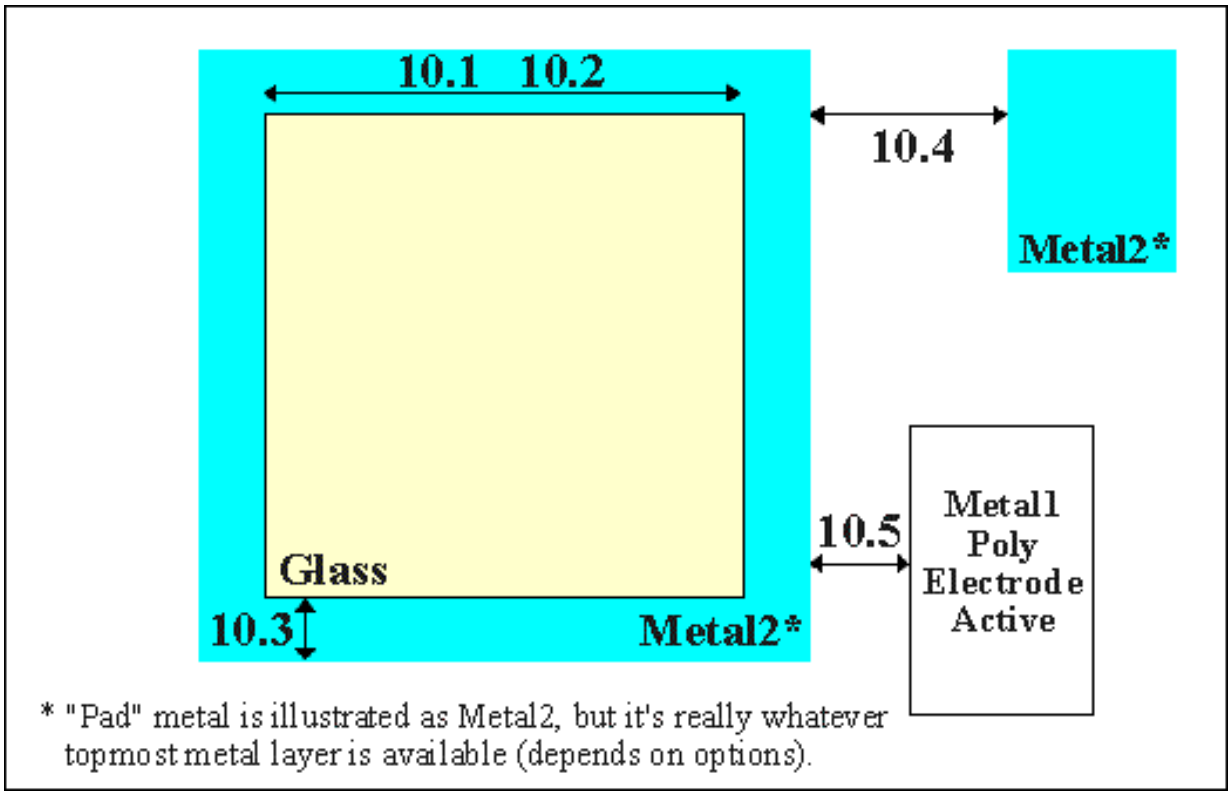
Rule	Description	Lambda
9.1	Minimum width	3
9.2.a	Minimum spacing	4
9.2.b	Minimum tight metal or SUBM spacing *(only allowed between minimum width wires - otherwise, use regular spacing rule)*	3
9.3	Minimum overlap of via1	1



SCMOS Layout Rules - Overglass

Note that rules in this section are in units of microns. They are not "true" design rules, but they do make good practice rules. Unfortunately, there are no really good generic pad design rules since pads are process-specific.

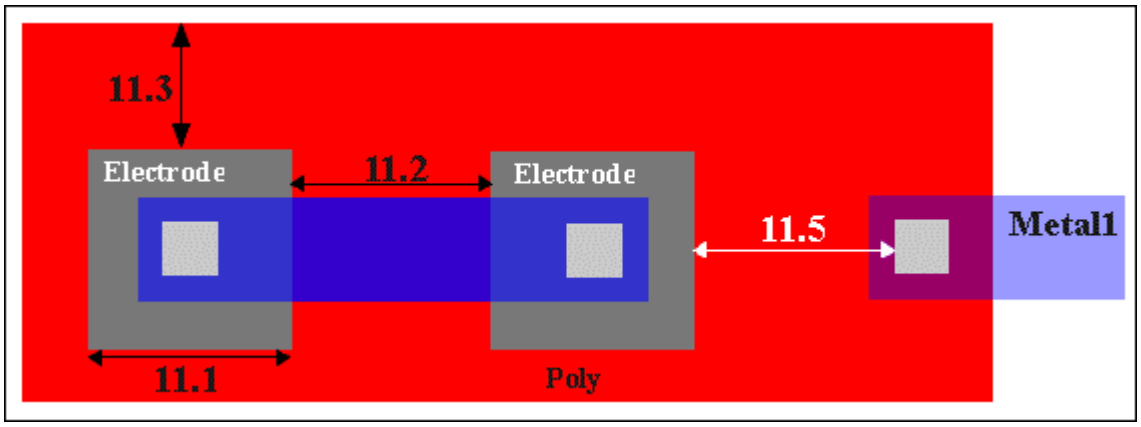
Rule	Description	Microns
10.1	Minimum bonding pad width	100 x 100
10.2	Minimum probe pad width	75 x 75
10.3	Pad metal overlap of glass opening	6
10.4	Minimum pad spacing to unrelated metal	30
10.5	Minimum pad spacing to unrelated active, poly or poly2	15



SCMOS Layout Rules - Poly2 (or Electrode) for Capacitor

The poly2 or electrode layer is a second polysilicon layer (physically above the standard, or first, poly layer). The oxide between the two polys is the capacitor dielectric. The capacitor area is the area of coincident poly and electrode.

Rule	Description	Lambda
11.1	Minimum width	3 [SUBM 7]
11.2	Minimum spacing	3
11.3	Minimum poly overlap	2 [SUBM 5]
11.4	Minimum spacing to active or well edge (not illustrated)	2
11.5	Minimum spacing to poly contact	3 [SUBM 6]
11.6	Minimum spacing to *unrelated* metal	2

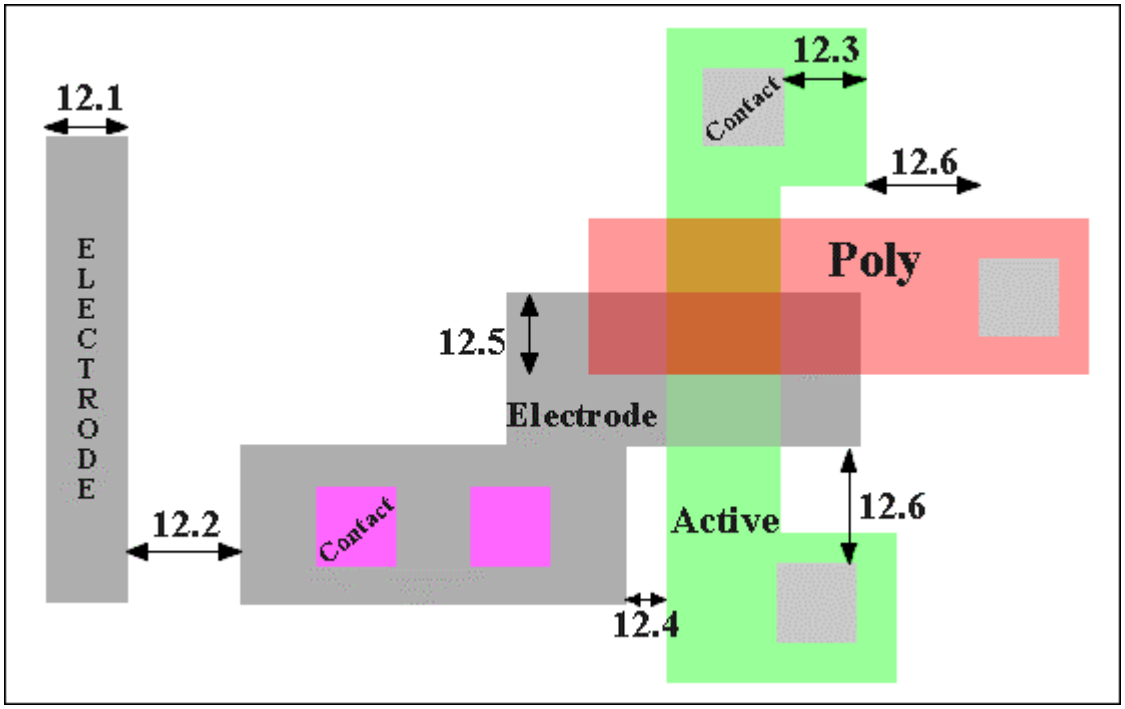


SCMOS Layout Rules - Electrode for Transistor

Same electrode (second poly) layer as for caps

Rule	Description	Lambda
12.1	Minimum width	2
12.2	Minimum spacing	3
12.3	Minimum electrode gate overlap of active	2
12.4	Minimum spacing to active	1
12.5	Minimum spacing or overlap of poly	2
12.6	Minimum spacing to poly or active contact	3

Table 19: SCMOS Layout Rules - Electrode for Transistor (Analog Option)

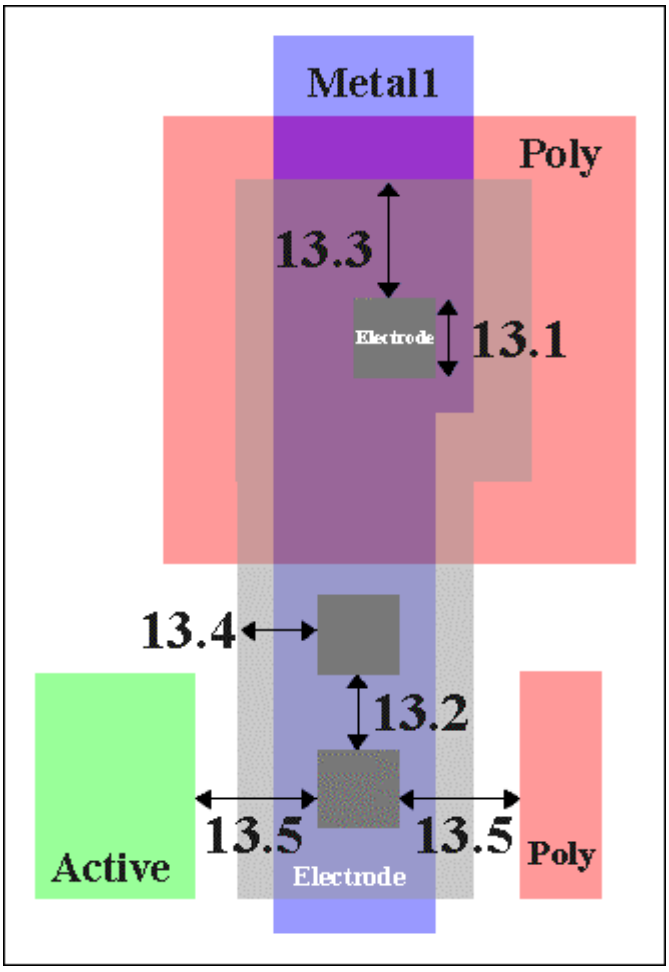


SCMOS Layout Rules - Electrode Contact

The electrode is contacted through the standard contact layer, similar to the first poly. The overlap numbers are larger, however.

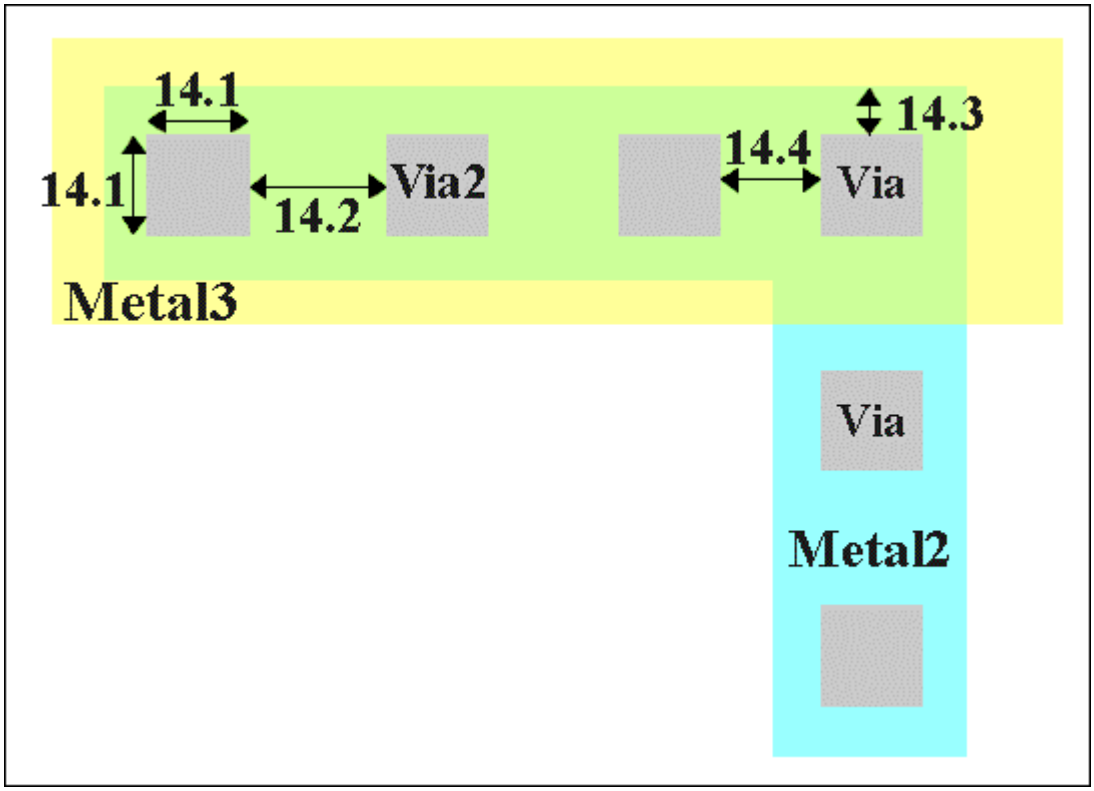
Rule	Description	Lambda
13.1	Exact contact size	2 x 2
13.2	Minimum contact spacing	2 [SUBM 3]
13.3	Minimum electrode overlap (on capacitor)	3
13.4	Minimum electrode overlap (not on capacitor)	2
13.5	Minimum spacing to poly or active	3

Table 20: SCMOS Layout Rules - Electrode Contact (Analog Option)



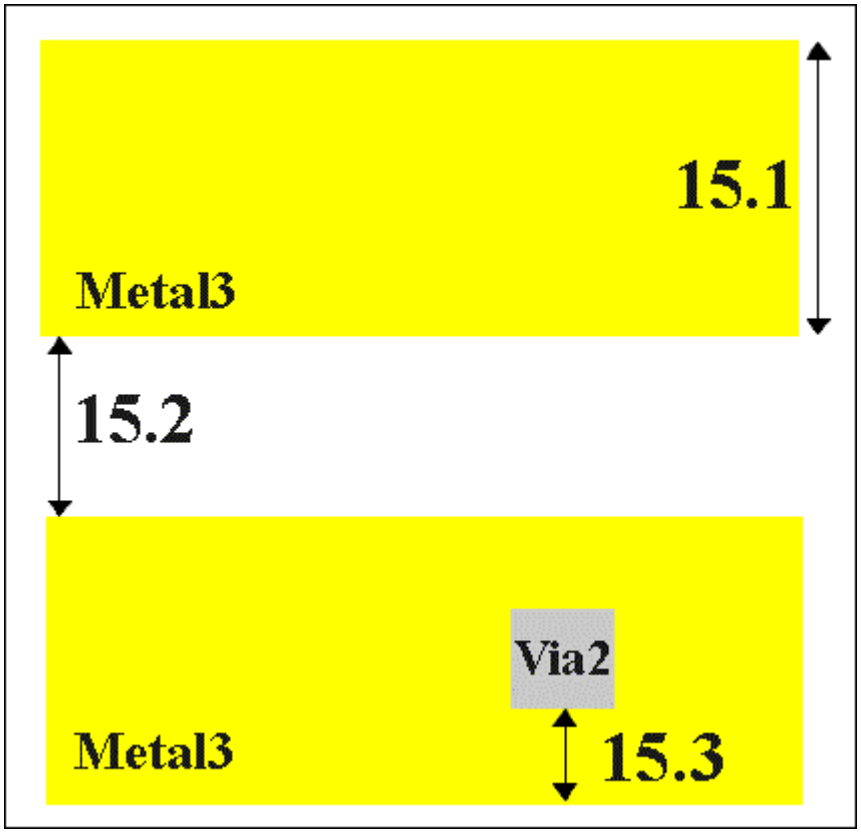
SCMOS Layout Rules - Via2

Rule	Description	Lambda
14.1	Exact size	2 x 2
14.2	Minimum spacing	3
14.3	Minimum overlap by metal2	1
14.4	Minimum spacing to via1	2
14.5	Via2 may be placed over contact	



SCMOS Layout Rules - Metal3

Rule	Description	Lambda
15.1	Minimum width	6 [SUBM 5]
15.2	Minimum spacing to metal3	4 [SUBM 3]
15.3	Minimum overlap of via2	2



SCMOS Layout Rules - High Res

(AMI 0.5 µ SC* designs only)

Rule	Description	Lambda
27.1	Minimum HR width	4
27.2	Minimum HR spacing	4
27.3	Minimum spacing, HR to contact (no contacts allowed inside HR)	2
27.4	Minimum spacing, HR to external active	2
27.5	Minimum spacing, HR to external poly2 (electrode)	2
27.6	Resistor is poly2 (electrode) inside HR; poly2 (electrode) ends stick out for contacts, the entire resistor must be outside well and over field	N/A
27.7	Minimum poly2 (electrode) width in resistor	5
27.8	Minimum spacing of poly2 (electrode) resistors (in a single HR region)	7
27.9	Minimum HR overlap of poly2 (electrode)	2