ECE 3421 – VLSI Design and Simulation, Spring 2013

Project
Design a Counter

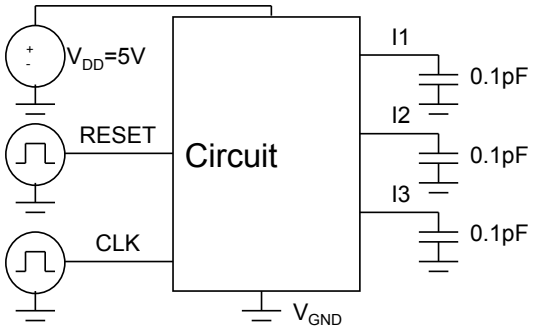
Design a counter that goes through the following sequence:
<I1, I2, I3>: 101, 000, 110, 111, 101, ... (repeats)

The inputs to the circuit are a CLK signal and a RESET signal. The outputs of the circuit are I1, I2, and I3. Each output I1, I2, and I3 drives a load of 0.1pF.

Use only NMOS and PMOS transistors in your design. Use VDD and VGND for power and ground lines for the transistors in your design. Use a power supply of 5V.

The goal is to minimize the (Energy $\times$ Delay) product for producing the sequence. You can set the CLK pulse width and period to whatever you like. On the falling edge of the clock, the outputs I1, I2, I3 must be valid with a full voltage swing. For example, if the correct output is "110", then I1 and I2 must be at 5V, and I3 must be at 0V. The (Energy $\times$ Delay) product is obtained by multiplying the total time required to go through the sequence with the total energy used during that time.

Simulation Setup



The simulation setup is shown above. The only parts that are to be used internal to the circuit are NMOS and PMOS transistors from the AMI05LIB. Your simulation should go for 6 clock cycles. In the first and last clock cycles, the RESET line will be high. In all the other clock cycles it will be low.

At the end of the first clock period (falling edge of CLK), the output should be reset to "101". At the end of the second period (falling edge of CLK), the output should be "000". Your circuit should go through the sequence: 101 (reset), 000, 110, 111, 101, 101 (reset). At the end of the 6th clock period, the output should be "101" since the reset is asserted. The time at the end of the 6th clock period is the total delay of your circuit.

Deliverables

Express all the values that you write with 2-digit precision using scientific notation.

- Plot of V_{clock}, I1, I2, and I3 versus Time (all three should be on the same plot). Mark the total delay on the plot. It will be equal to 6 times whatever you chose as your clock period (if your clock period is 10ns, then total delay is 60ns).
- Calculate the total energy (point at the end of the 6th clock period). Show your plots.
- Diagram of your circuit (with transistors and their sizes labeled).
- Zip your project folder (that contains your cadence files) under ece3421 directory. Provide this zip file to us via email.
- Specify your simulation input (vpulse) setup. You may use screenshots for this.
- 2-3 page report describing your design strategy and results. What did you do to minimize the delay? What did you do to minimize power? How did your results change when you tried different sizes of transistors or different gate implementations?

Grading

- 1/2 points for correctly functioning design
- 1/4 points for optimality of (Energy $\times$ Delay) product
- 1/4 points for report