ECE 3421 – VLSI Design and Simulation, Spring 2013

Lab Assignment 4
Layout

1. Introduction

This lab will introduce you to the Cadence layout tools. You will layout a CMOS inverter using AMI 0.5 μm technology.

2. Cadence Layout Tools

[STEP 1:] Start the Cadence software as usual. In the CIW windows, go to Tools → Technology File Manager and a Technology File Tool Box will appear. Click Attach and a New Technology Library window will appear as in Figure 1. Choose your ece3421 Design Library and the NCSU_TechLib_ami06 Technology Library.

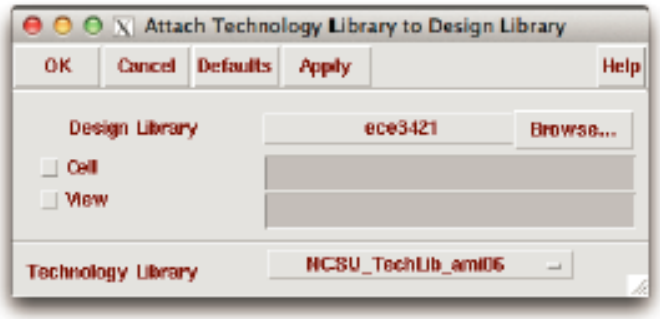

Figure 1: Attach Technology Library window.

[STEP 2:] In the CIW window, go to File → New → Cellview and a CreateNew File window appears. Set the Library Name to ece3421, your design library name, and Cell Name to INV. For Tool, choose Virtuoso, and the View Name of "layout" will be automatically added for you, as shown in Figure 2.

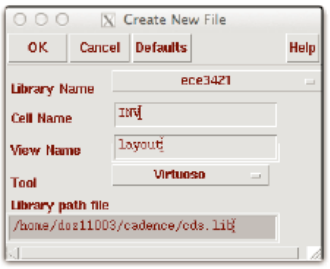

Figure 2: Attach Technology Library window.

At this time, you will see two windows appear, one is the Layer Selection Window (LSW), and the other is the Virtuoso Editing window, shown in Figure 3. To make the develop environment more convenient, we can setup the display through Option → Display, set the minor spacing to 0.3, major spacing to 1.5, X snap spacing to 0.15, and the Y snap spacing to 0.15.Thus, the layout would be on grids and the grid distance is λ (0.3μm).

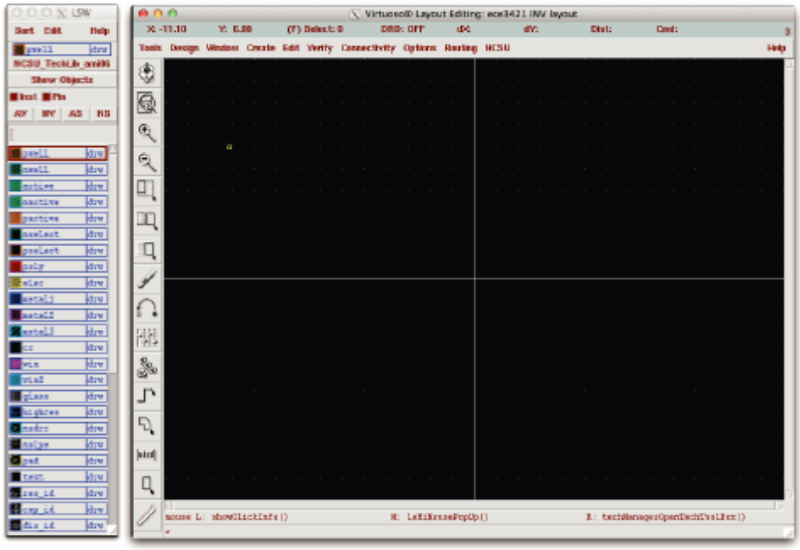

Figure 3: LSW and Virtuoso windows.

[STEP 3:] Drawing the N-diffusion (Active). Select “active” layer from LSW window, and go to Create → Rectangle in the Virtuoso Editing window, drawing a box as shown in Figure 4. When creating the rectangle for this step and for all subsequent steps, you will need to follow the AMI 0.5 Design Rules (see SN05_Rules.pdf) You should periodically check that you are conforming to the design rules by going to Verify → DRC.

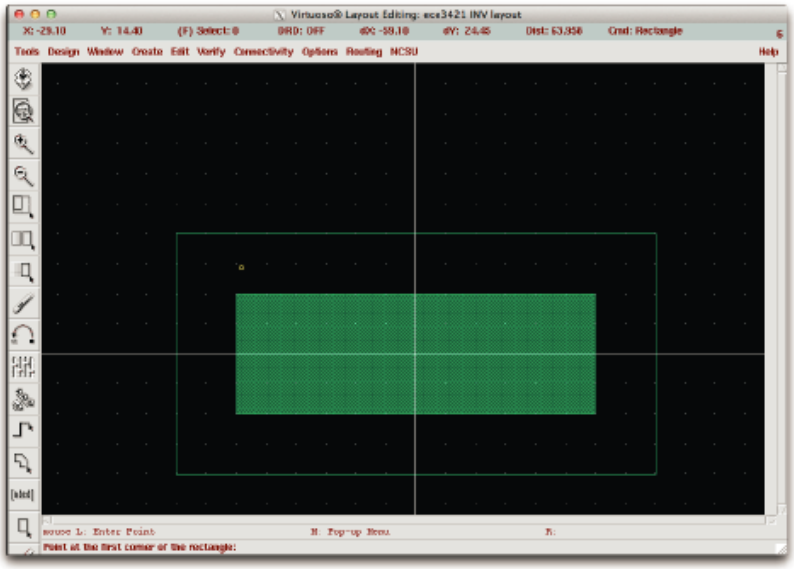

Figure 4: The N-diffusion (Active) Box.

[STEP 4:] Drawing the Gate Poly. Select ”poly1” layer from LSW window, and go to Create → Rectangle in the Virtuoso Editing window, drawing a gate box as shown in Figure 5.

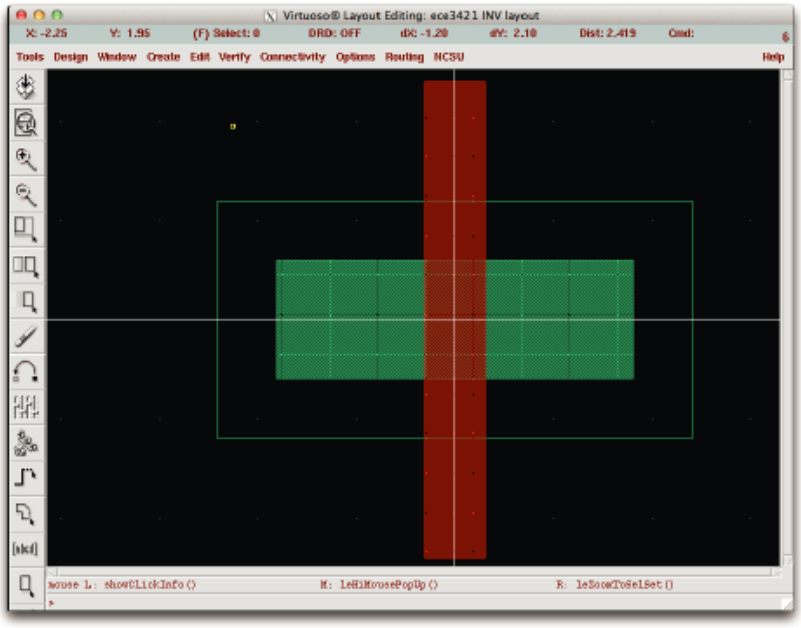

Figure 5: Gate Poly Rectangle.

[STEP 5:] Making Active Contacts. Select the "cc" layer from LSW window, and go to Create → Rectangle in the Virtuoso Editing window, drawing two contact squares as shown in Figure 6. The contacts must be exactly 0.6μm by 0.6μm. You can always set the exact size and position through Edit → Properties after select the item you want to modify.

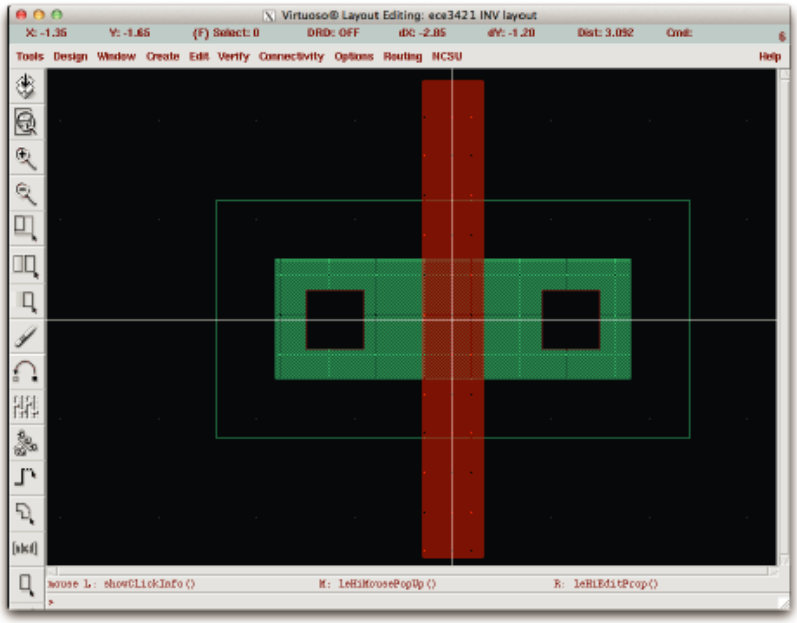

Figure 6: Active Contact Blocks.

[STEP 6:] Covering Contacts with Metal-1 and drawing an "Nselect" layer. Select "metal1" layer from LSW window, and go to Create → Rectangle in the Virtuoso Editing window, drawing two metal-1 covering boxes. Then select nselect layer from LSW window, and then turn to the Create → Rectangle in the Virtuoso Editing window, drawing a rectangle extending over the active region by 0.6 μm in all directions, as shown in Figure 7.

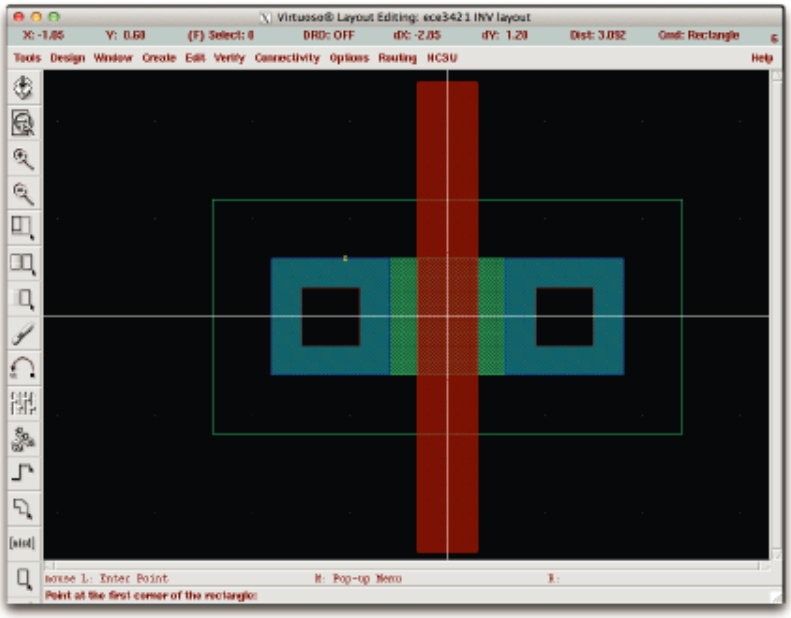

Figure 7: NMOS layout.

[STEP 7:] Drawing a PMOS transistor. Repeat STEP 5-8 to draw a PMOS transistor, using a “pselect” layer instead of a “nselect” layer. You should end up with a layout as shown in Figure 8. The pMOS transistor is above the nMOS transistor.

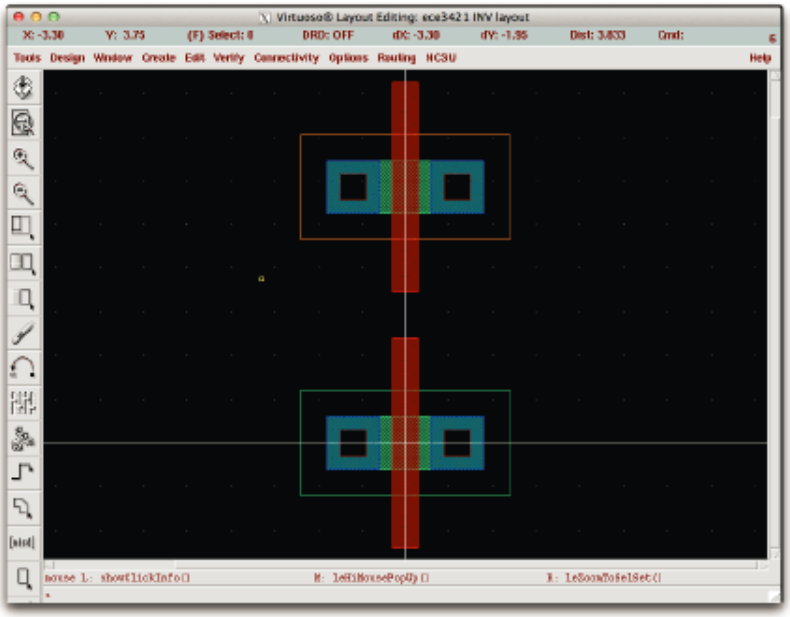

Figure 8: Drawing the layout of PMOS.

[STEP 8:] Drawing the N-Well. Select “nwell” layer from LSW window, and go to Create $->$ Rectangle in the Virtuoso Editing window, drawing a N-Well square as shown in Figure 9.

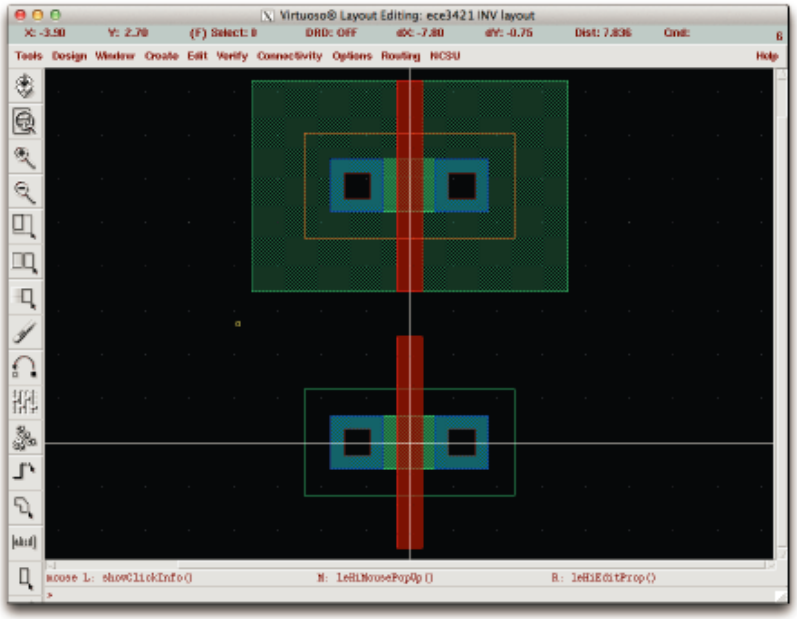

Figure 9: Layout of NMOS and PMOS transistors.

[STEP 9:] Connecting the Output and Inputs of the inverter. Use a "metal1" layer to connect the drains of the NMOS and PMOS transistors and use a "poly1" layer to connect the gates as shown in Figure 10. Note that the transistors are completely symmetric and the source and drain regions are interchangeable.

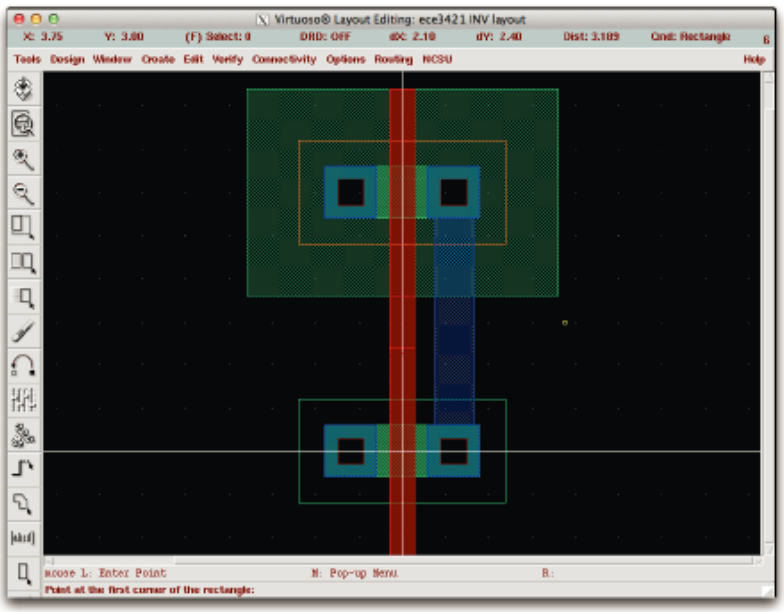

Figure 10: Connecting the drains of NMOS and PMOS.

[STEP 10:] Make a Metal-1 connection for the Input as shown in Figure 11. Note that you must have a poly square completely surrounding the contact by 0.3μm.

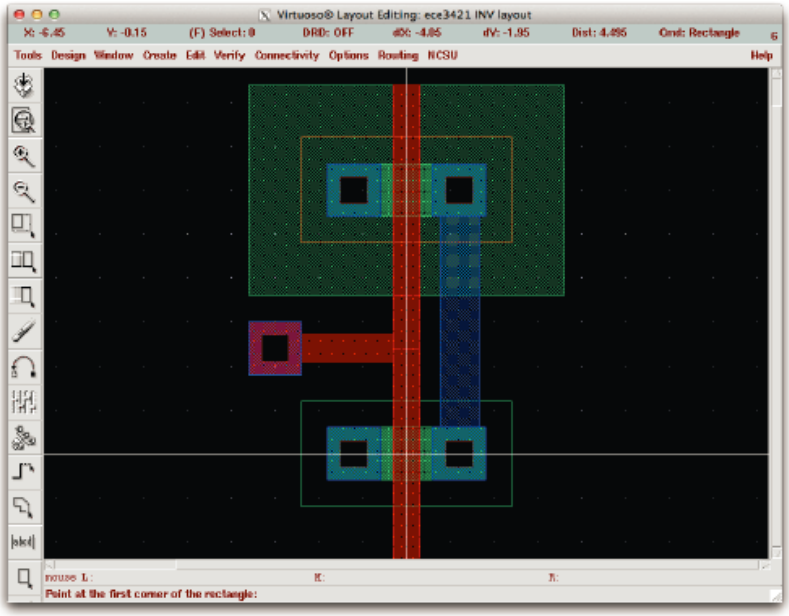

Figure 11: Making a Metal-1 connection for the Input.

[STEP 11:] Drawing the Power and Ground rails in Metal-1. Select ”metal1” layer from LSW window, and go to Create → Rectangle in the Virtuoso Editing window, drawing metal-1 box for the power and ground rails as shown in Figure 12.

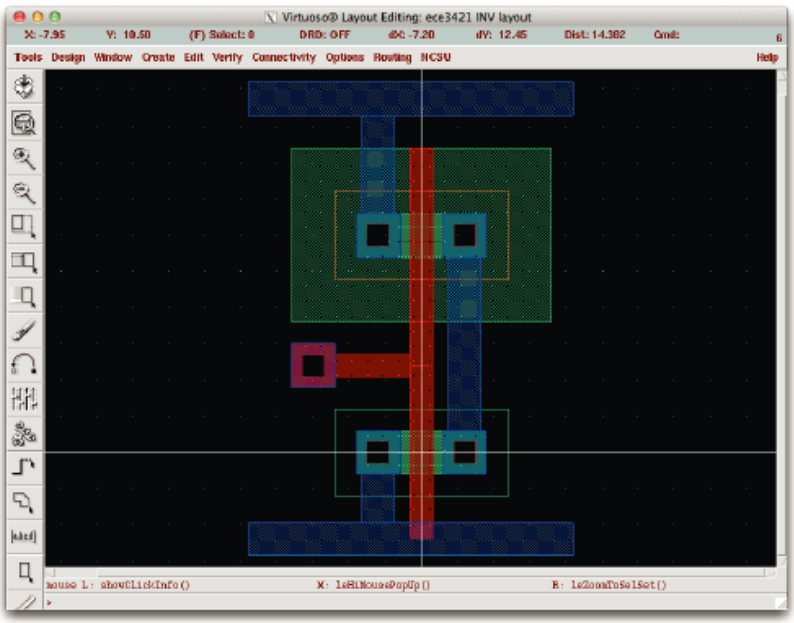

Figure 12: The Power and Ground Rails in Metal-1.

[STEP 12:] Substrate contacts. As in Figure 13, draw a p-select square next to the NMOS transistor, then draw an active inside the p-select region. Draw the active contact square inside the p-type active region, and finally make a metal connection to ground. For N-substrate contact, draw an n-select square next to the PMOS transistor, then draw an active inside the n-select region. Draw the active contact square inside the n-type active region, and finally make a metal connection to vdd.

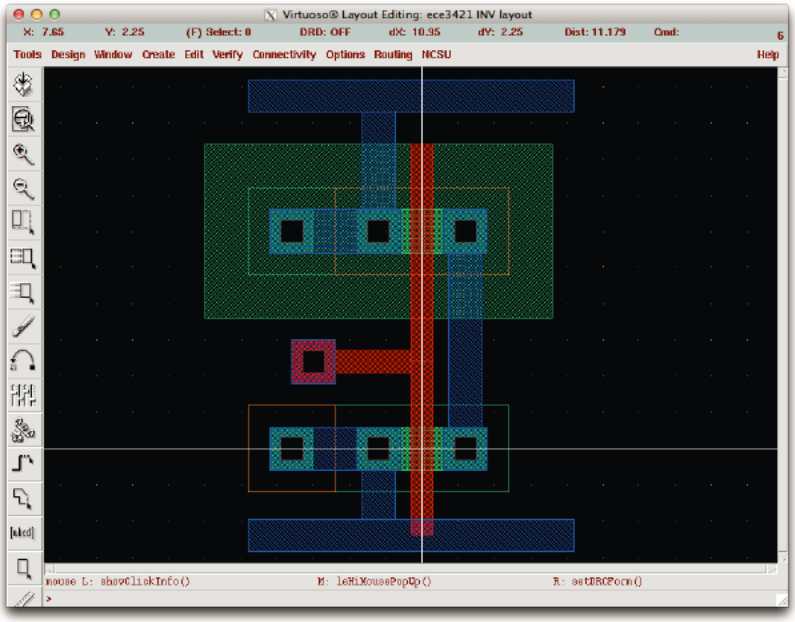

Figure 13: Substrate contact.

[STEP 13:] Run a DRC check and an LVS check to confirm that the layout conforms to the design rules and also matches the inverter schematic. See LVS.pdf for instructions on LVS verification.

NOTE: You might have to change your schematic to remove the variables like pPar("Wp"), since LVS might fail if they aren't actual numbers, and you'll got CDF parameter errors even you've assigned value in CDF window.

[STEP 14:] After you make sure your design passes DRC and LVS, merge all the blocks for the same layer by selecting the entire design and then going to Edit $\rightarrow$ Merge.

[STEP 15:] Make a copy of files further needed and clean all the person information, close all the active windows and now you've finished all the contents of Lab-4 of ECE 3421.

Assignment

1. Using the same techniques you used to create the inverter, draw the layout for a 2-input NAND gate, and hand it in. Make sure that the layout passes DRC and LVS. You will need to create a NAND gate schematic in order to run LVS.