ECE 3421 – VLSI Design and Simulation, Spring 2013

Lab Assignment 2
Delay analysis of an Inverter

1. Introduction

This lab will introduce you to concepts of performance characterization of an inverter circuit.

2. Create Parameterized Symbol

You are now going to modify the symbol from Lab 1 so that it can be parameterized so that you can modify the transistor parameters at the symbol level. This will allow you to change transistor parameters without having to descend into the hierarchy and also removes the need to create multiple inverters for different sizing requirements.

[STEP 1:] Start icfb and in the CIW window go to Tools → CDF → Edit. An Edit Component CDF window will open up. Fill it in as shown in Figure 1. The Cell Name should be the same as the name you used in Lab 1, you may also use the browse button.

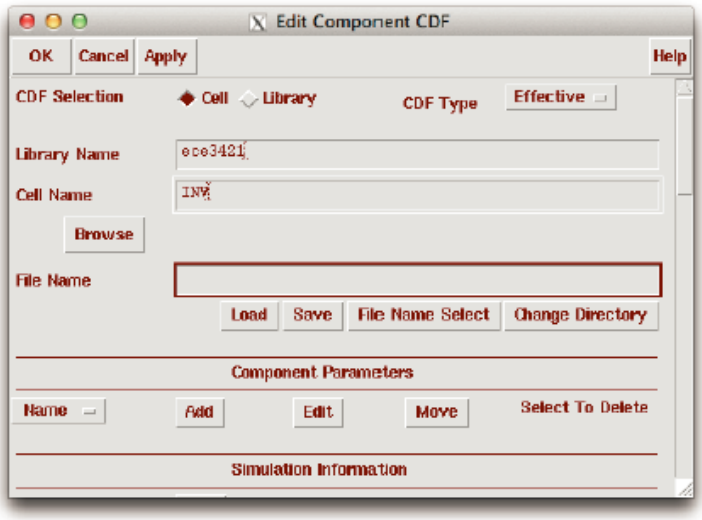

Figure 1: Edit Component CDF window.

[STEP 2:] Click the Add button under Component Parameters, and the Add CDF Parameter window will appear. Fill in the window as shown in Figure 2 and then click OK to add Wn and prompt for "nMOS Width".

[STEP 3:] Repeat Step 2, to add a parameter named Wp and a prompt of "pMOS Width".

[STEP 4:] Click OK in the Edit Component CDF window. From the CIW window, open the INV Schematic from Lab 1.

[STEP 5:] Select the nMOS transistor and edit its width property as shown in Figure 3. The pPar function will retrieve the parameter value from CDF Parameter we created in Step 2.

[STEP 6:] Repeat Step 5, to change the pMOS width property to pPar("W").

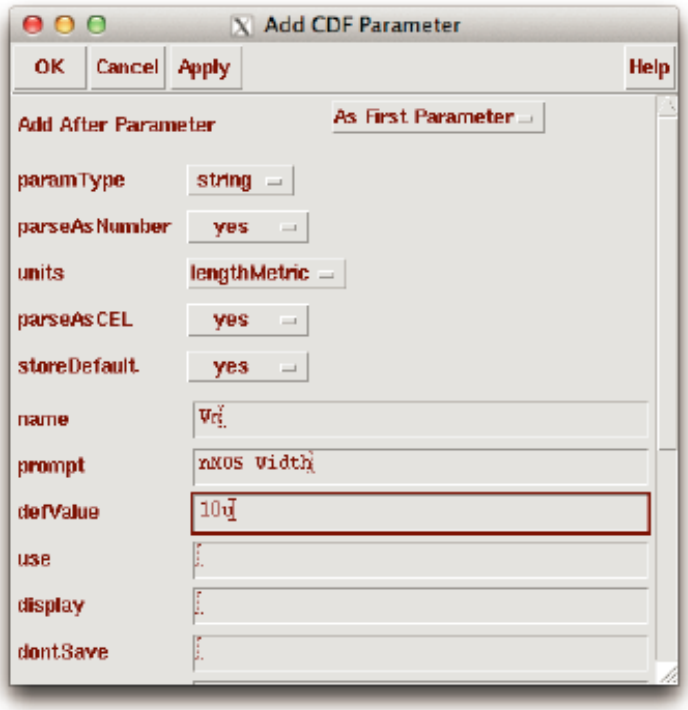

Figure 2: Add CDF Parameter window.

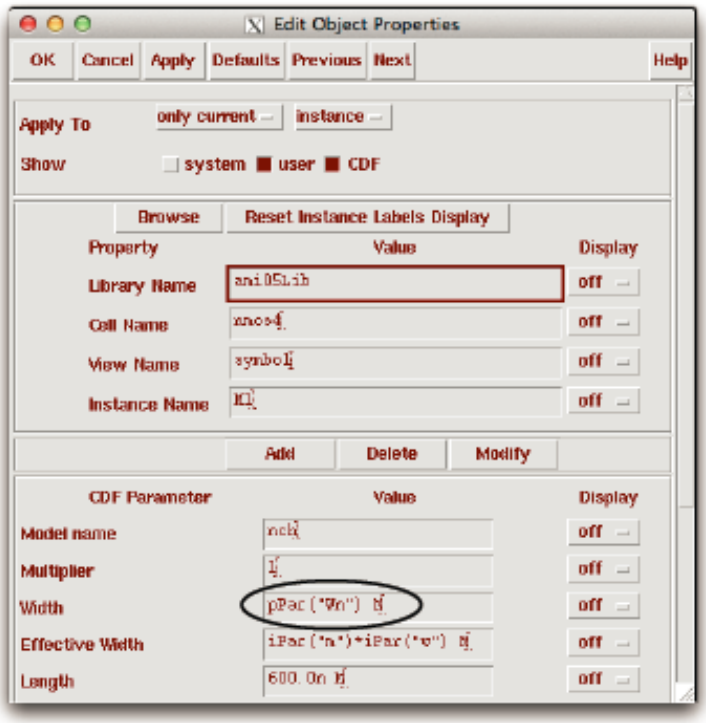

Figure 3: Edit nMOS properties.

3. Delay Measurement

[STEP 1:] Create a new Cellview Schematic in the ece3421 library named lab2.

[STEP 2:] Create the following schematic as shown in Figure 4. It should be similar to the testinv schematic from Lab 1. Set the properties of the vpulse to make a 5V square wave. You will need to change the fall and rise times to 1f s. Also change the pulse width to 10 ns.

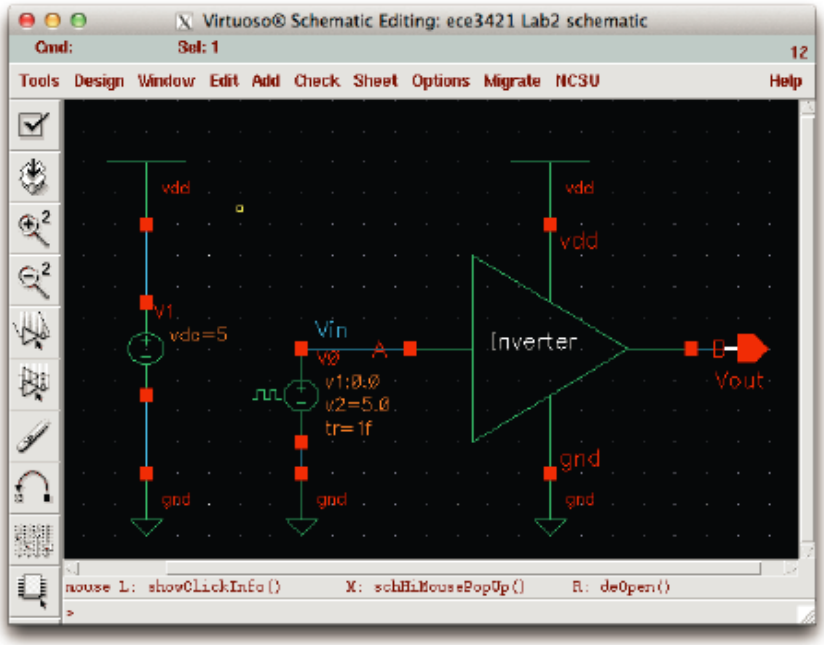

Figure 4: Single inverter.

[STEP 3:] Using Analog Environment, plot the input and output waveforms. Finish problem 1.
[STEP 4:] Add a 2pF capacitor from the analogLib library in Passives to the output as shown in Figure 5.

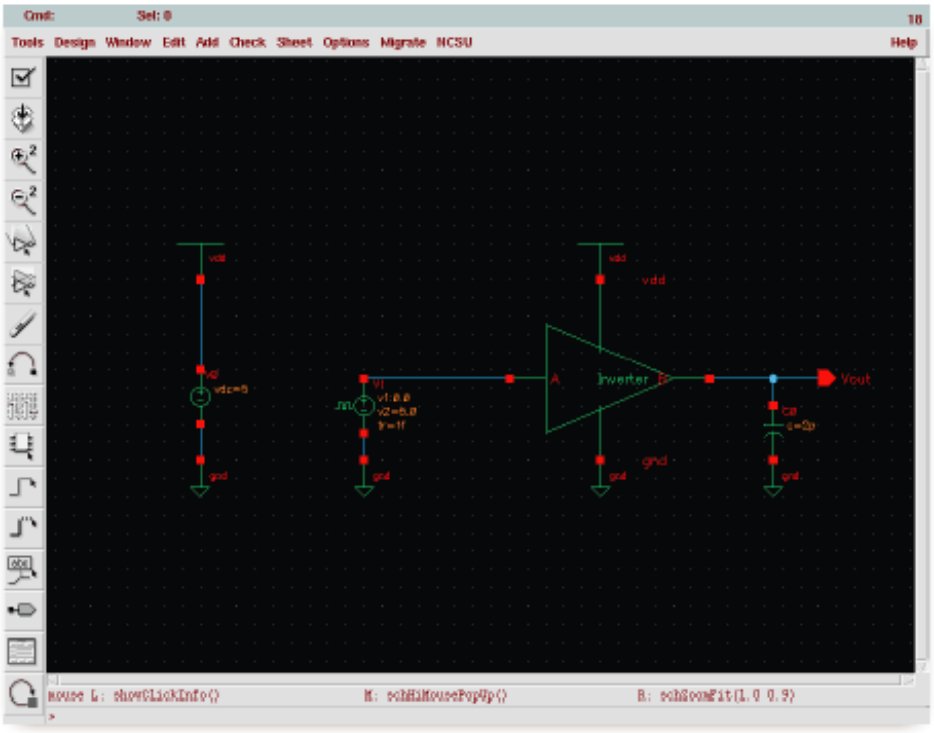

Figure 5: Single inverter with capacitor

[STEP 5:] Using Analog Environment, plot the input and output waveforms. You may finish problem 2-5.
[STEP 6:] Add a second inverter as shown in Figure 6. For both inverters, adjust the pMOS width to the value you arrived

at above so that both inverters are balanced. Finish problem 6-11.

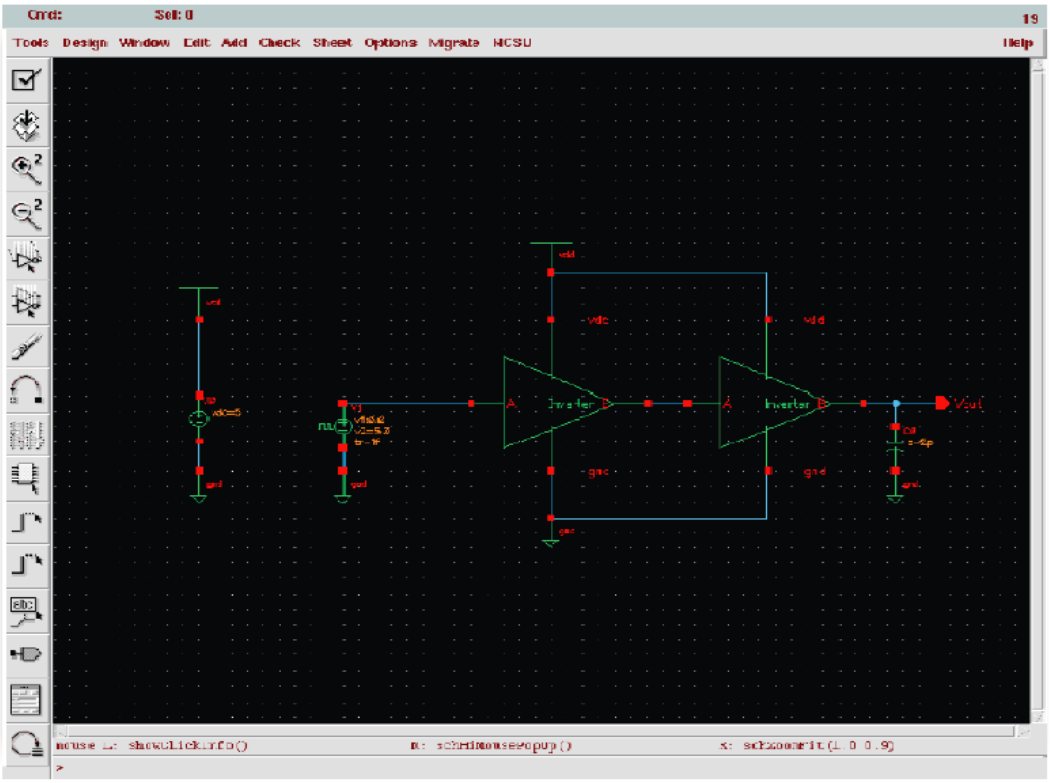

Figure 6: Two inverters with capacitor.

[STEP 7:] Exit the Analog Circuit Design Environment Simulation window, and then exit the Virtuoso Schematic Editing window.

[STEP 8:] In the CIW window, go to File → Exit. Make a copy of files further needed and clean all the person information. And now you've finished all the contents of Lab-2 of ECE 3421

Assignment

1. Measure the rise and fall delay times from the vpulse to VOUT. Remember that the delay time is the time from 50% input to 50% output. Hand in a printout of the waveform for one period of the input along with the delay measurements.
2. For the inverter with a 2pF capacitor, measure the rise and fall delay times from the vpulse to VOUT. Hand in a printout of the waveform for one period of the input. Mark clearly the delay measurements.
3. Comment on why the delay times changed from an inverter without load to an inverter driving a 2pF load?
4. Why are the rise and fall delay times different for an inverter with 2pF load?
5. What should be the width of the pMOS transistor so that the delay times are equal? Show how you arrived at this value. Hand in a printout of the output waveform for this balanced inverter driving a 2pF load. Mark clearly the delay measurements.
6. For the two-inverter configuration, measure the rise and fall delay times from the vpulse to the input of the second inverter. Hand in a printout of the waveform for one period of the input. Mark clearly the delay measurements.
7. Why has the delay time changed for the first inverter?
8. For the two-inverter configuration, measure the rise and fall delay times from the vpulse to VOUT. Hand in a printout of the waveform for one period of the input. Mark clearly the delay measurements.
9. Change the cap to 8pF, how has this changed the delay from vpulse to VOUT? Does the circuit work as expected? Why or why not? Hand in the output waveform.
10. Adjust the size of the second inverter to minimize the delay of the two inverters and show how you arrived at that value. You must keep the inverter balanced. Hand in the output waveform for the minimum delay.
11. Is it possible to size the second transistor to equalize the delay to the 2pF case? Why or why not?