ECE 3421 – VLSI Design and Simulation, Spring 2013

Lab Assignment 1
Design and Simulation of an Inverter

1. Introduction

This lab aims at introducing you to the Cadence software on the Sun workstation. First, a list of basic UNIX commands is given, and then followed by setting the UNIX environment for the Cadence design tools. Finally, a simple example of simulating a CMOS Inverter is presented.

2. Basic Unix Commands

`http://linuxdevcenter.com/linux/excerpt/LinuxPG_quickref/linux.pdf`.

3. Setting up an Account to Run the Cadence Tools

You will need to login a Linux workstation and set up your Linux environment to run the Cadence software. After you login, open up a terminal window by right clicking on the desktop and then choosing Tools $->$ Terminal. This will open up a shell window. Depending on when your account was created, you may be using csh as your default login shell. The current recommended shell for ECS users is bash. To check if you are using, type "echo $shell" at the shell prompt. If the reply is "/bin/csh", you will need to change to use the bash shell by typing "exec bash" at the shell prompt. Once you have established that you are using bash, proceed with the following steps to setup the Cadence tools.

- –$ mkdir cadence
- –$ mkdir inbox
- IMPORTANT: The following command will overwrite your .bashrc file in your home directory. If you have something important in your .bashrc file, save it to a temporary file.

  –$ bash /apps/ecs-apps/software/ece/cdssetup/cdsupdate2007

  Add your .bashrc changes from the temporary file back, if necessary.
- –$ source ∼/.bashrc

4. Starting Cadence Software

- –$ cd ∼/cadence

  (Make sure the current directory is cadence every time you open Cadence)
- –$ icfb &

  A Command Interface Window (CIW) will appears on the screen shortly after the starting window of Cadence, as shown in Figure 1. You should leave this window open all the time, since the content of cadence.log file will show up here, and you may also need to check the status of operations through this window from time to time.

Figure 1: Main window (CIW) of the Cadence tools.

5. Remote Access to Cadence

In order to access remotely, a X-windows tool is needed. Online help can be found at

`http://www.engr.uconn.edu/~yfei/teaching/uconncds/usr/setup.html`

6. Creating Inverter Schematic

[STEP 1:] In the CIW window, go to File → New → Library, a Create Library window appears as below. Fill out the pop-up form according to Figure 2, and click OK.

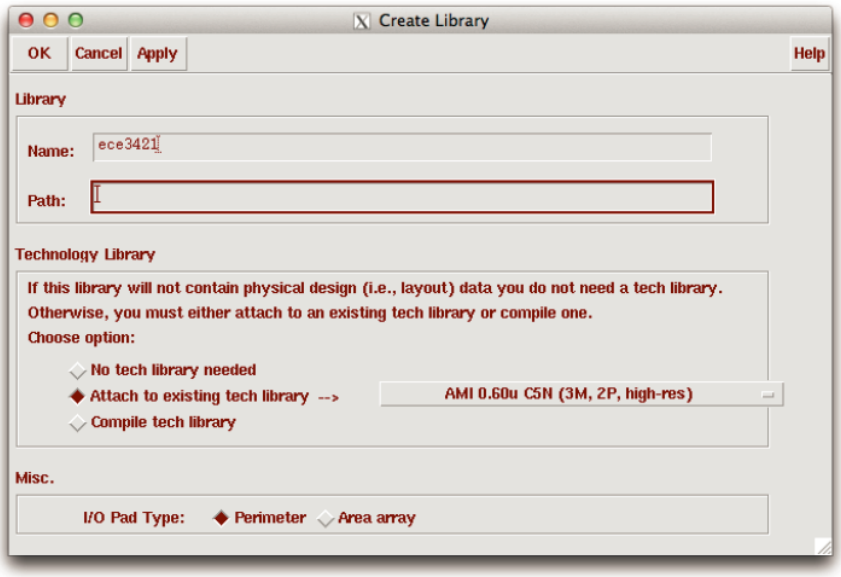
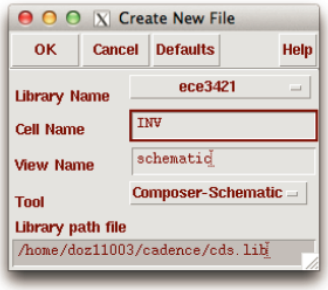
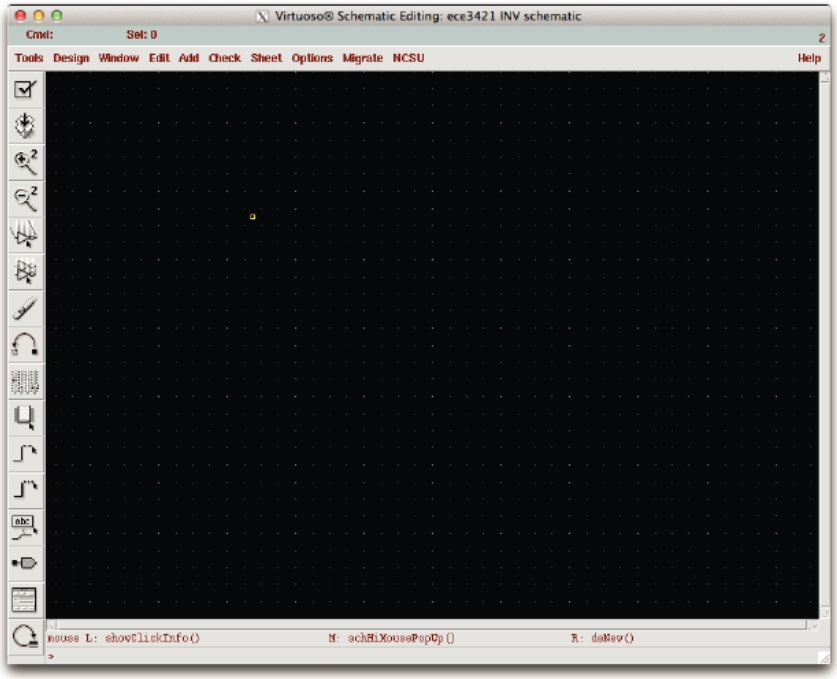


Figure 2: Creating a new library.

[STEP 2:] In the CIW window, go to File → New → Cellview, A Create New File window appears like Figure 3a. Fill it out accordingly and click OK. Then a new Virtuoso Schematic Editing window appears as in Figure 3b.



(a) Creating a new file.



(b) The Virtuoso Schematic Editing window.

Figure 3: Creating and editing a new schematic.

[STEP 3:] In the Virtuoso Schematic Editing window, go to Add → Instance. An Add Instance window and a Component Browser window appears as shown in Figure 4 and Figure 5a.

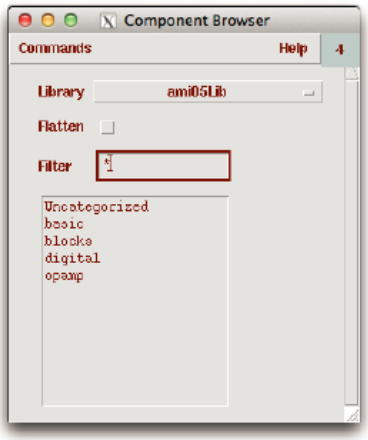
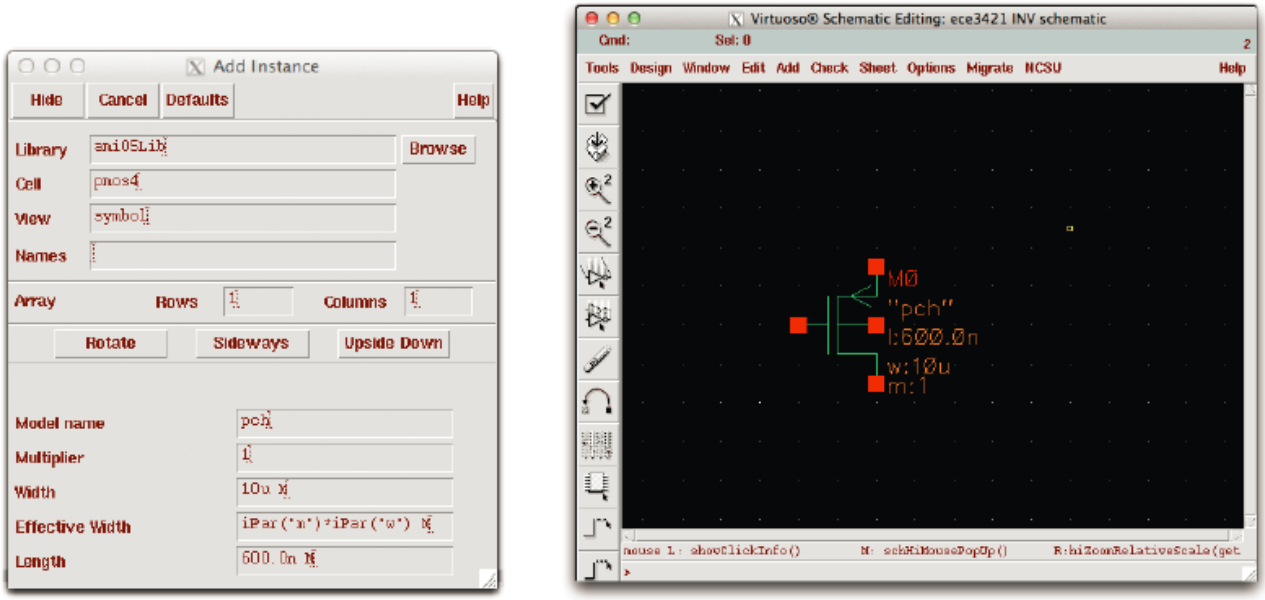


Figure 4: Instance window.

[STEP 4:] Select AMI05LIB[1] in Library, PMOS4 in Cell, and SYMBOL in View. And the Add instance window should now have the PMOS information filled in as in Figure 5a. If not, correct the information accordingly. Then Stamp a PMOS device symbol in the Virtuoso Schematic Editing window by double click on the place to put, as shown in Figure 5b.



(a) Add instance window

(b) Stamping PMOS device.

Figure 5: Adding instance window and stamping a PMOS device.

[STEP 5:] Repeat STEP 3 & 4 for an NMOS4 transistor.

[STEP 6:] In the Virtuoso Schematic Editing window, go to Add → Pin. Name the pin "A", direction set to input as shown in Figure 6.

[1] If there isn't a ami05Lib in the library browser window, then just add the library with follow steps: In CIW window, go to Tools → Library Path Editor; In the Editor window, go to Design → Add Library. Finally, in the Add Library window, go to /apps/ecs-apps/software/ece/AMSLib/AMI05/ami05Lib in Directory and select the ami05Lib in the Library, click OK to finish adding and the ami05Lib shown in Labrary Path Editor, save & close the window.

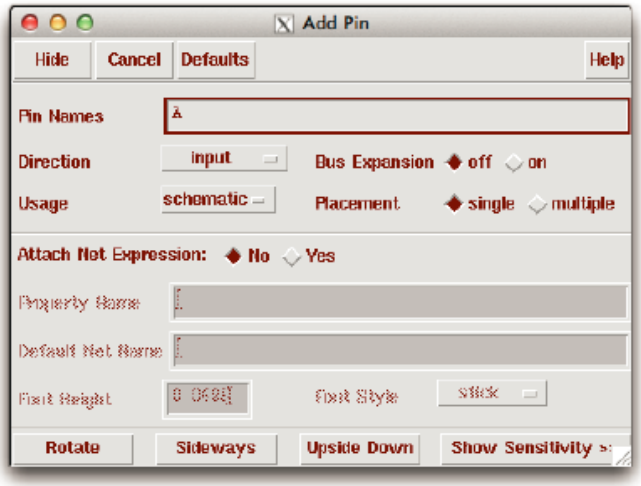


Figure 6: Adding a New Pin.

[STEP 7:] Repeat STEP 6 for a pin named “B”, direction set to output; A pin named “vdd”, direction set to input; And a pin named “gnd”, direction set to input.

[STEP 8:] Check each pin, make sure that pins “A”, “vdd”, and “gnd” have the direction set to input and pin “B” has the direction set to output. If not, the properties can be edited by going to Edit → Properties → Object.

[STEP 9:] In the Virtuoso Schematic Editing window, go to Add → Wire and connect the instances as shown in Figure 7.

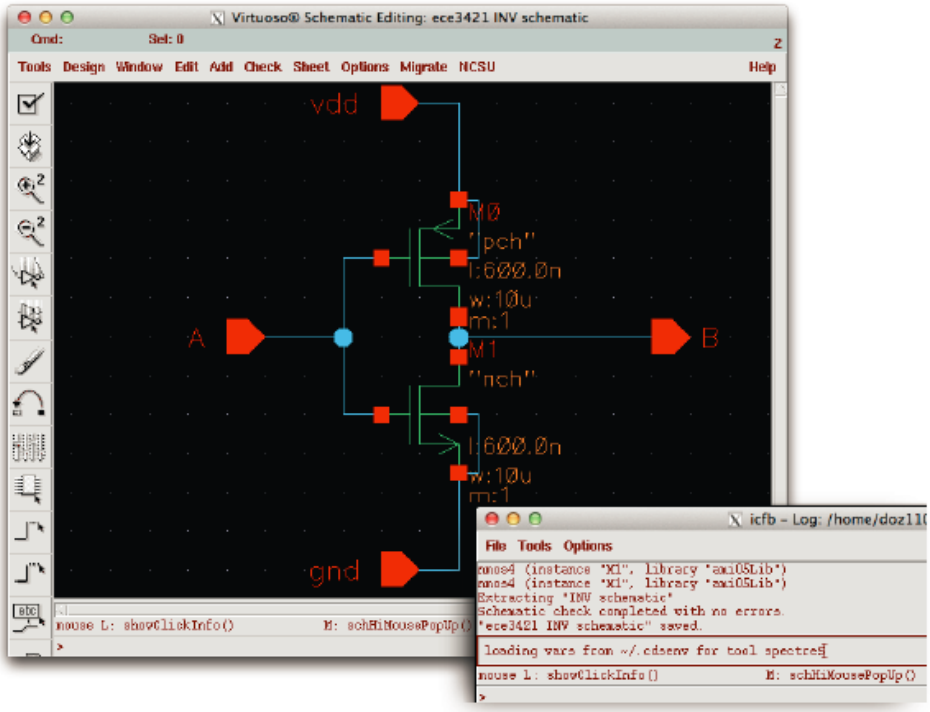


Figure 7: Inverter schematic and CIW information for checking.

[STEP 10:] In the Virtuoso Schematic Editing window, go to Design → Check and Save. You should have no errors or warnings when checking the CIW window. As shown in the bottom right window in Figure 7.

7. Symbol Creation of Sub-Circuits in Cadence

If a design is complicated, generally we use the top-down design method, or hierarchy structure. In this case, it is very beneficial to assign each sub-circuit a corresponding symbol (or icon) to represent that module. This step largely simplifies the schematic representation of the overall design. Thus, the SYMBOL view of a circuit module is an icon that stands for

the collection of all components within the module.

[STEP 1:] In the Virtuoso Schematic Editing window, go to Design → Create Cellview → From Cellview, the following window Figure 8 will pop up.

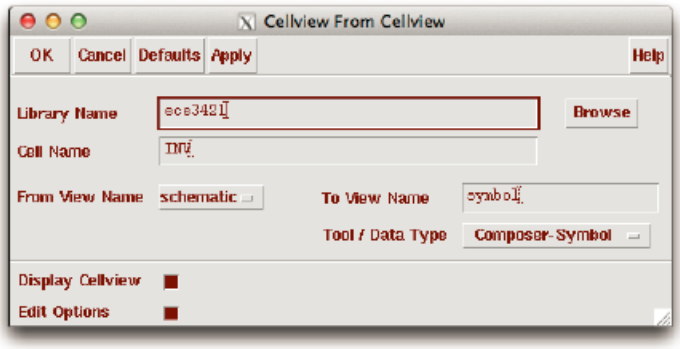


Figure 8: Cellview From Cellview form.

[STEP 2:] Check the view names and click OK. Make sure that the target view name is symbol, which is indicated in "To View Name". And check the following settings with Figure 9 below.

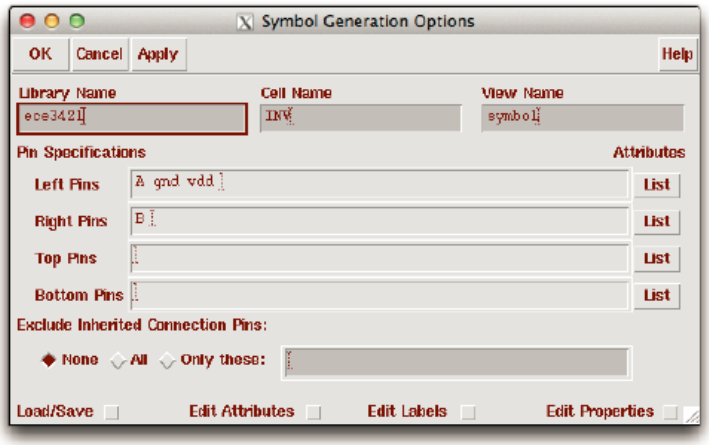


Figure 9: Symbol Generation Options form.

[STEP 3:] In a new window, a symbol is automatically generated. The default shape of the symbol icon is a rectangle as shown in Figure 10.

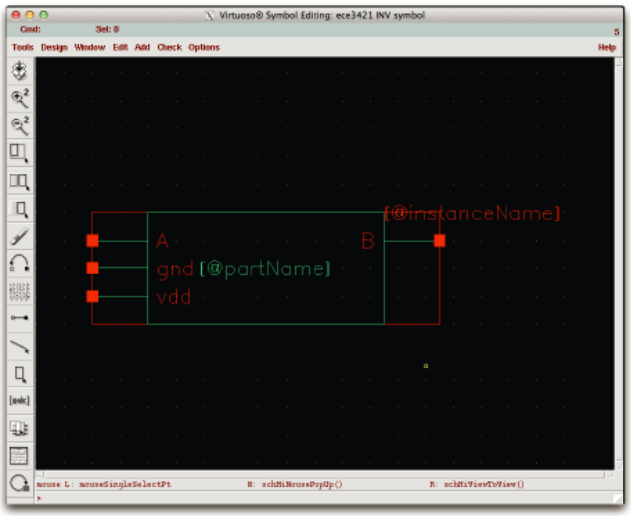


Figure 10: Automatically generated inverter symbol.

[STEP 4:] Editing the shape of the symbol icon. You can do the following operations on your symbol: Deleting/replacing some existing parts; Adding new geometric shapes; Changing the locations for pins and instance name; Adding new labels; The commands can be find under Add and Edit menus, to draw the shape you want ,simply use line under shape in the Add menu, for instance.Pay attention to the top left corner, the content of cmd indicates the current editing mode. Figure 11 shows an example of a manually created Inverters symbol, obtained by editing the symbol above.

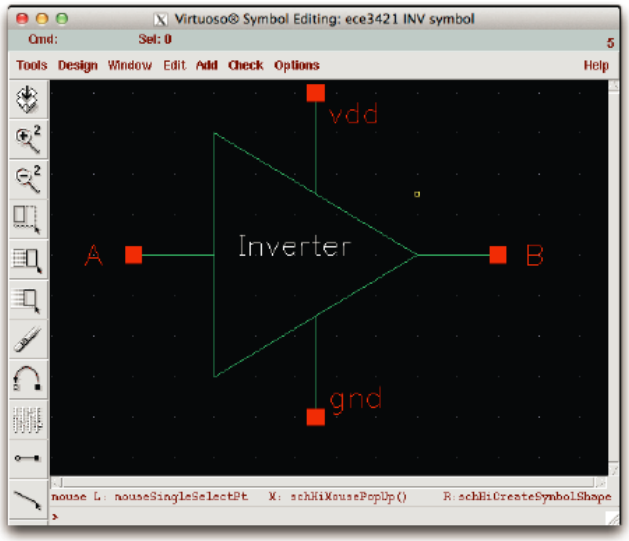


Figure 11: The inverter symbol after modification.

[STEP 5:] In Virtuoso Symbol Editing window, go to Design → Save. Thus, created our own symbol for future use.
[STEP 6:] In CIW window, go to Tools → Library Manager, as shown in Figure 12.

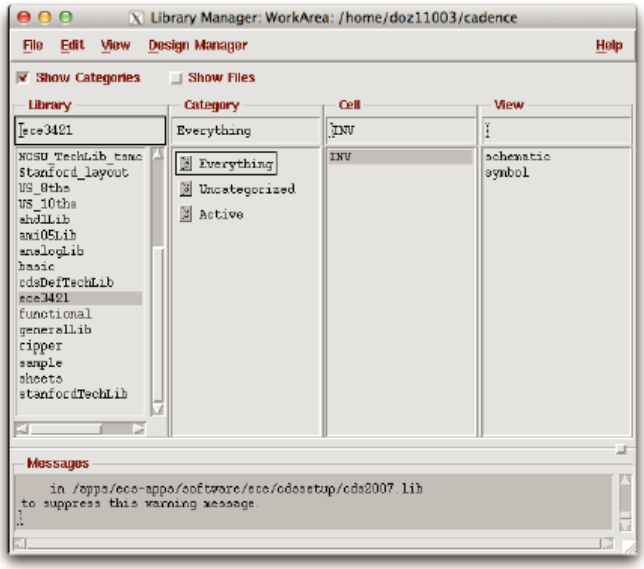


Figure 12: The Library manager.

[STEP 7:] In Library Manager window, check Show Categories option. Click on the library created before.
[STEP 8:] In Library Manager window, go to Edit → Categories → New, as shown in Figure 13.
[STEP 9:] In New Category Window click on INV and click the right arrow and rename the category “Active”, click OK.

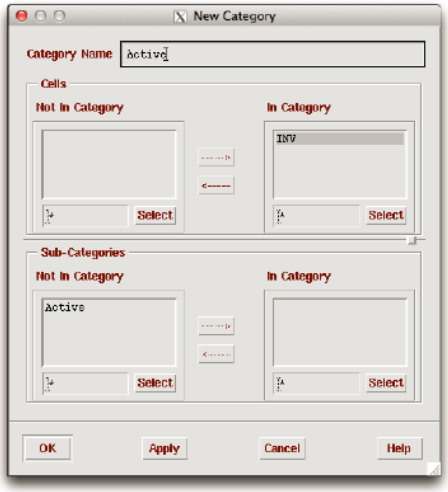


Figure 13: The New Category Window.

8. Simulation using DC analysis

Now we are going to simulate the inverter we just created to confirm that it operates as we expect.

[STEP 1:] In the CIW window, go to File → New → Cellview. A Create New File window appears. Fill it out according to Figure 14 and click OK. Then a new Virtuoso Schematic Editing window appears as we already know.

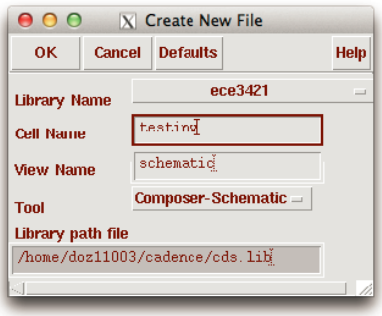


Figure 14: Creating the test file.

[STEP 2:] Add an instance of the new INV symbol that we just created, as shown in Figure 15.

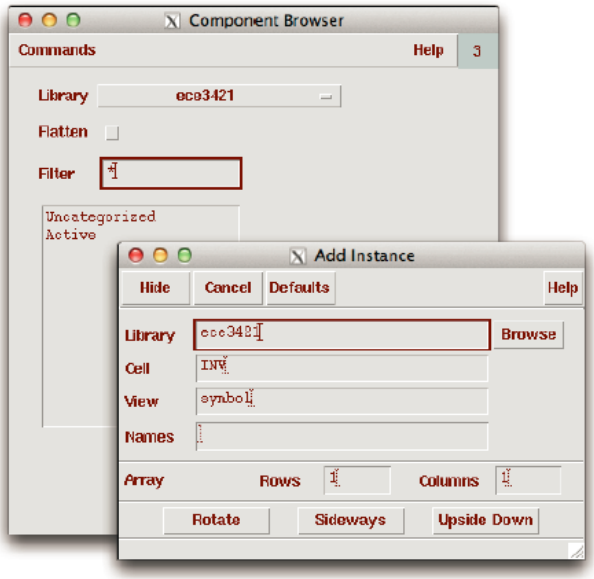


Figure 15: Main window (CIW) of the Cadence tools.

[STEP 3:] Add a vdc instance from the analogLib library with DC voltage set to 0V, and Number of noise/freq. pairs to 0. Set the properties the same as in Figure 16. This vdc is used to connect Vin and gnd.

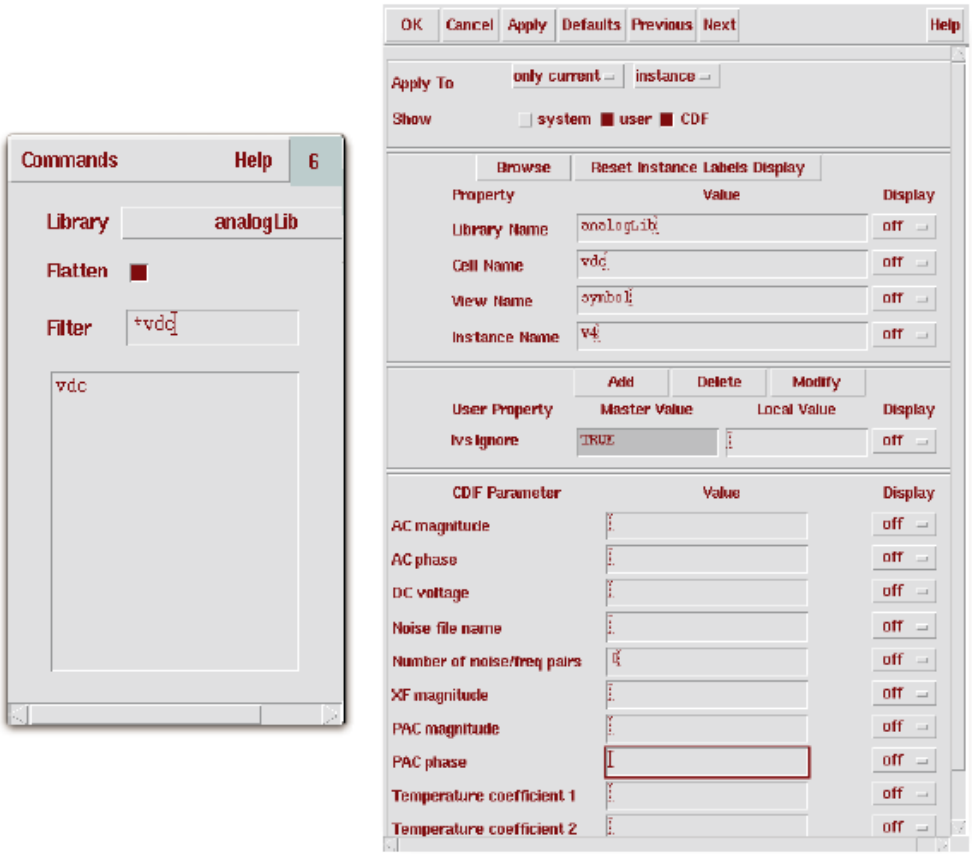


Figure 16: Adding vdc & Properties of vdc.

[STEP 4:] Add another vdc, with DC voltage set to 5V. This vdc is used to connect vdd and gnd.

[STEP 5:] Add an output pin named Vout.

[STEP 6:] In Virtuoso Schematic Editing window, go to Add → Wire, connecting all the components refer to Figure 18. The vdd and gnd symbols are also in the analogLib library.

[STEP 7:] In the Virtuoso Schematic Editing window, go to Add → Wire Name, name the input wire to the inverter Vin. So that we can assign input & output with name Vin & Vout in the following steps.

[STEP 8:] In the Virtuoso Schematic Editing window, go to Design → Check and Save. Correct any errors in your schematic figure. Check the CIW window for error information as shown in Figure 17.

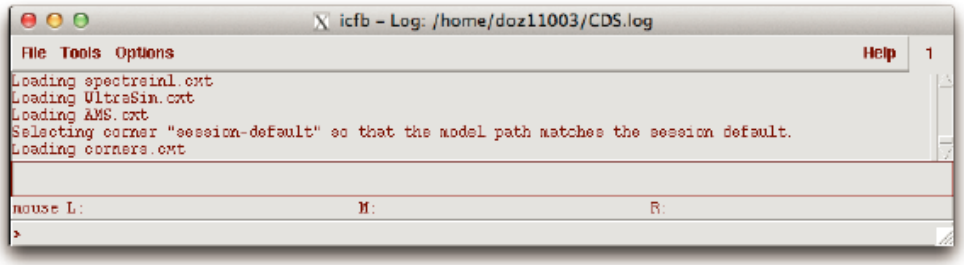


Figure 17: Main window (CIW) of the Cadence tools.

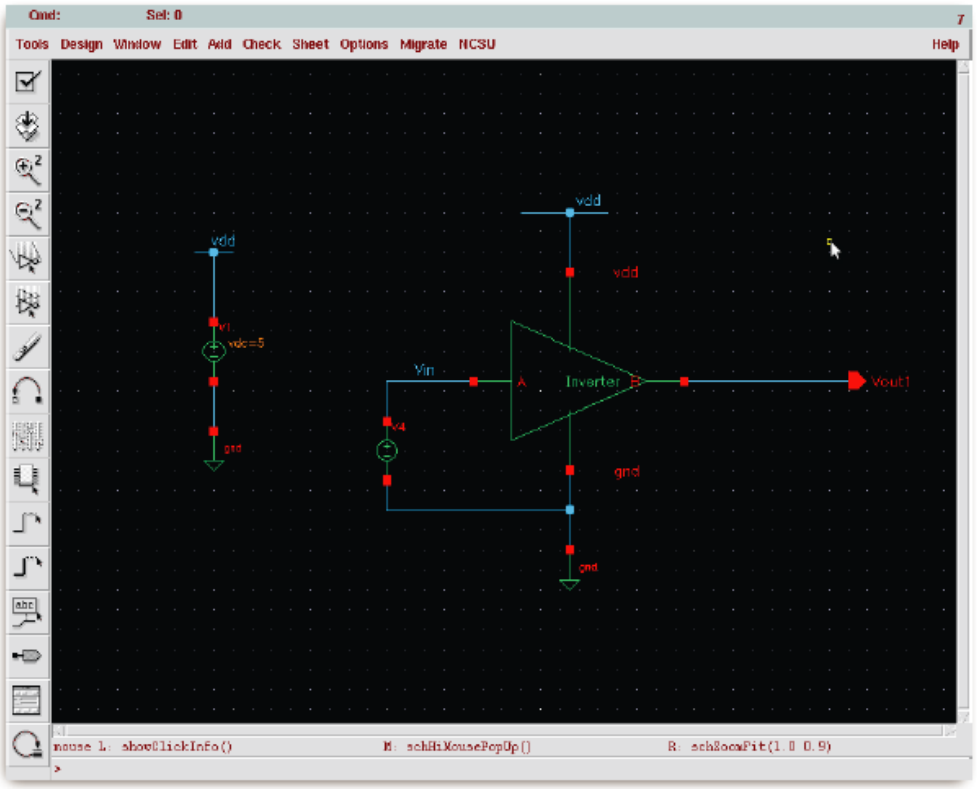


Figure 18: The completed testinv schematic for DC analysis.

[STEP 9:] In the Virtuoso Schematic Editing window, go to Tools → Analog Environment, an Analog Circuit Design Environment window would appear as shown in Figure 19.

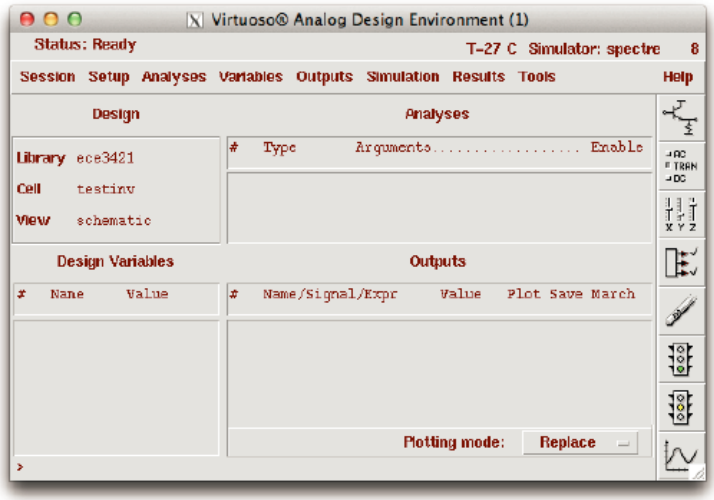


Figure 19: Analog Circuit Design Environment window.

[STEP 10:] In the Analog Circuit Design Environment window, go to Setup → Model Libraries, a Model Library Setup window appears. Click the Browse button and choose the models directory, and then choose the ami05.scs model. Click Add, now as in Figure 20, click OK.

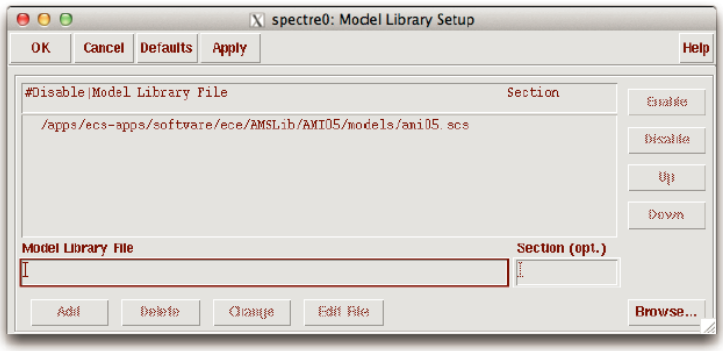


Figure 20: Adding model path.

[STEP 11:] In the Analog Circuit Design Environment window, go to Analysis → Choose. Fill out the form according to Figure 21. Choose Component Parameter, then click Select Component,select the vdc connected to Vin from the schematic, then select dc.

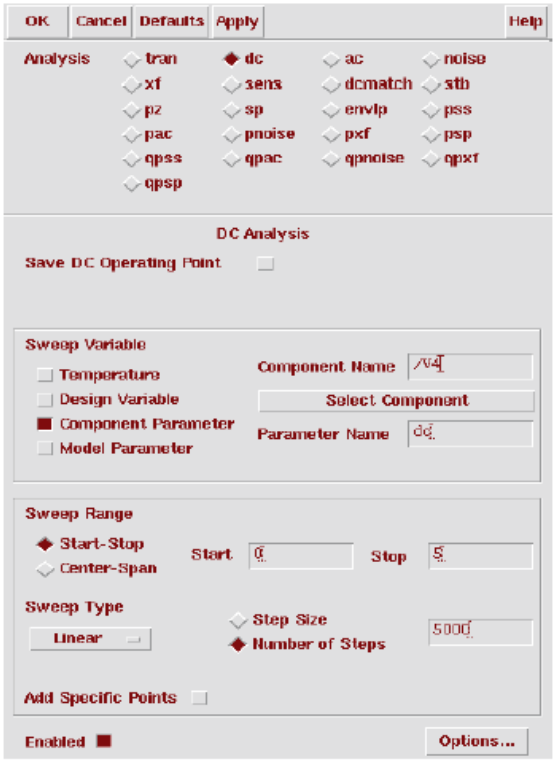


Figure 21: Setting up DC analysis.

[STEP 12:] In the Analog Circuit Design Environment window, go to Outputs → To be Plotted → Select on Schematic. Then go back to the testinv schematic window and select the Vin and Vout wires. Note, the wires should change color after selected, and the signals should be added in the outputs window as in Figure 22.

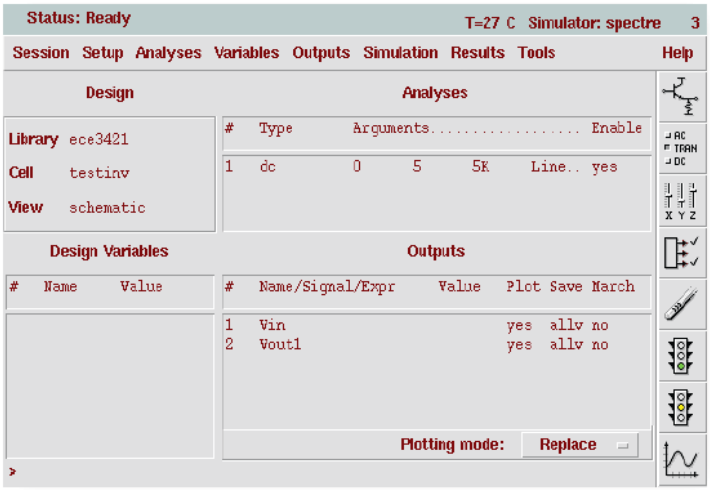


Figure 22: Analog Circuit Design Environment ready for a simulation.

[STEP 13:] In the Analog Circuit Design Environment window, go to Simulation → Netlist and Run. The plot of the simulation should appear in a Waveform Window, like Figure 23. Add a marker to see the switching threshold. Save the plot with marker for the report, and finish problem 1.

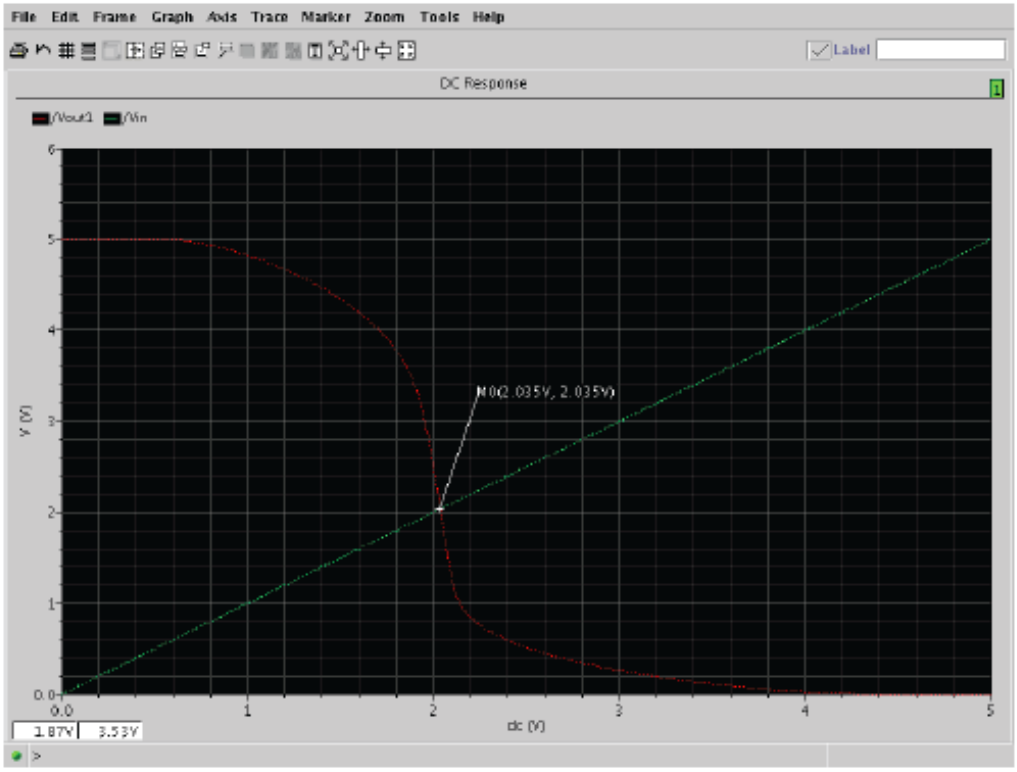


Figure 23: testinv simulation result.

9. Simulation using transient analysis

[STEP 1:] Change the vdc, which connects to Vin, to a vpluse from analogLib under sources under independants library. Set the properties the same as in Figure 24.

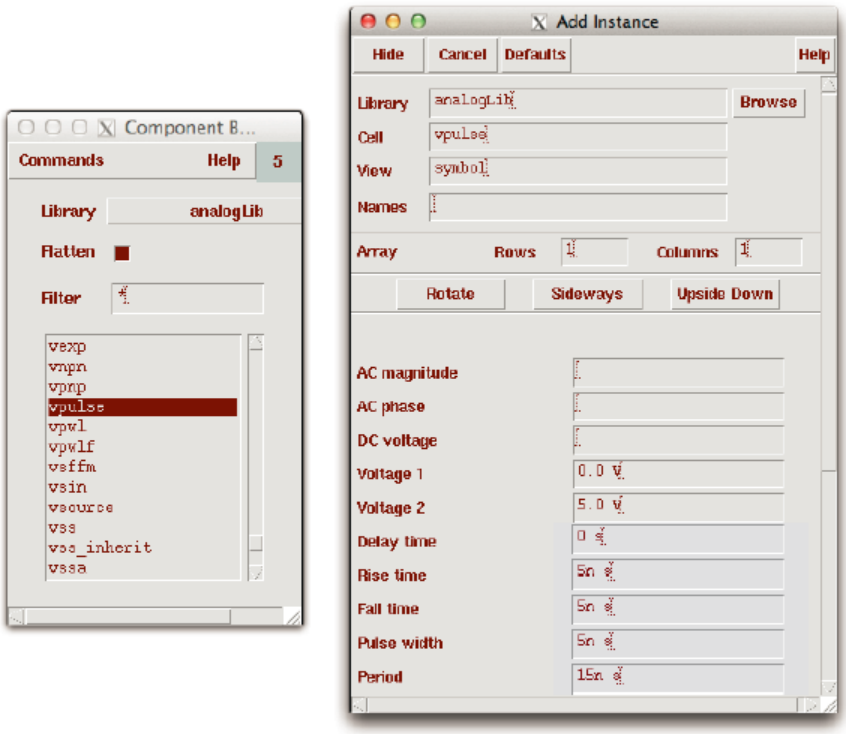


Figure 24: Adding vpulse & Properties of vpulse.

[STEP 2:] In the Virtuoso Schematic Editing window, go to Design → Check and Save. The schematic should look like Figure 25. Correct any errors in your schematic figure. Check the CIW window for error information as shown in Figure 26.

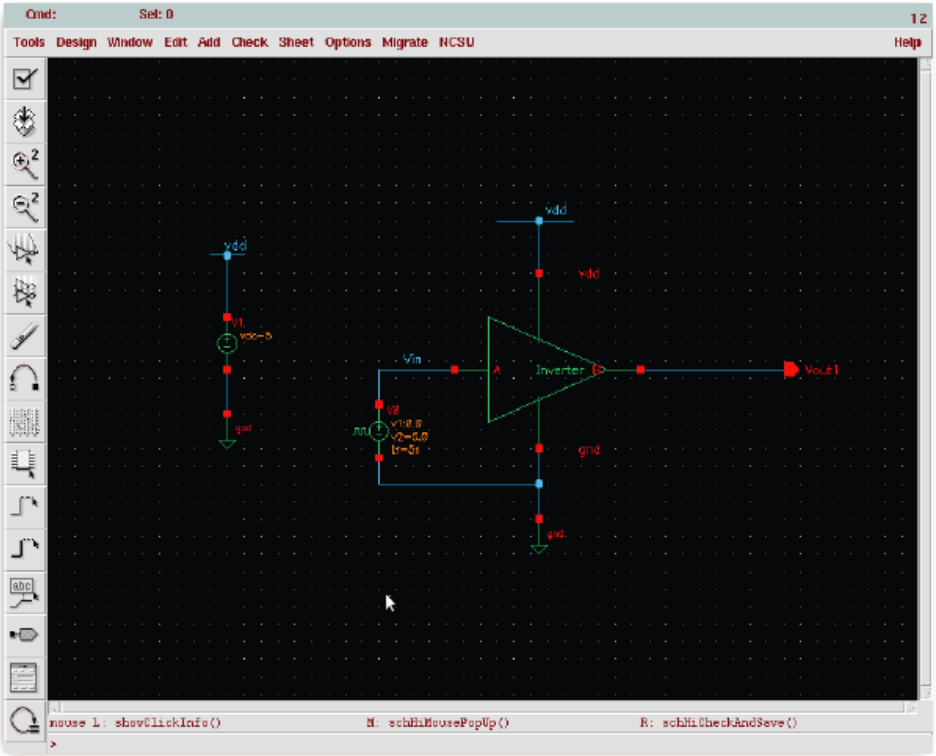


Figure 25: The completed testinv schematic for transient analysis.

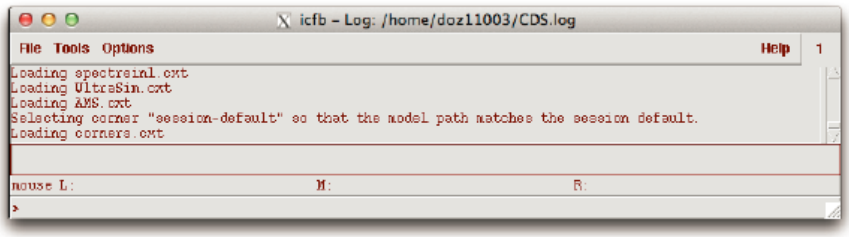


Figure 26: Main window (CIW) of the Cadence tools.

[STEP 3:] In the Virtuoso Schematic Editing window, go to Tools → Analog Environment, an Analog Circuit Design Environment window would appear as shown in Figure 27.

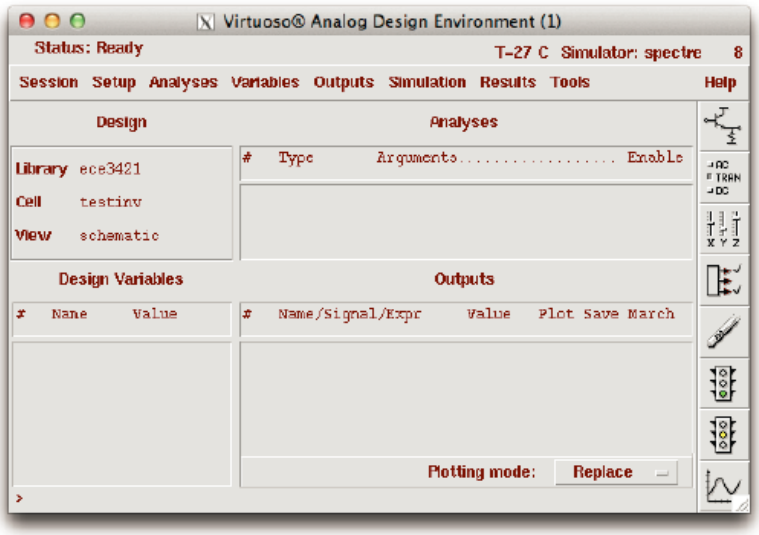


Figure 27: Analog Circuit Design Environment window.

[STEP 4:] In the Analog Circuit Design Environment window, go to Setup → Model Libraries, a Model Library Setup window appears. Click the Browse button and choose the models directory, and then choose the ami05.scs model. Click Add, now as in Figure 28, click OK. (This is needed every time that a new simulation session is started.)

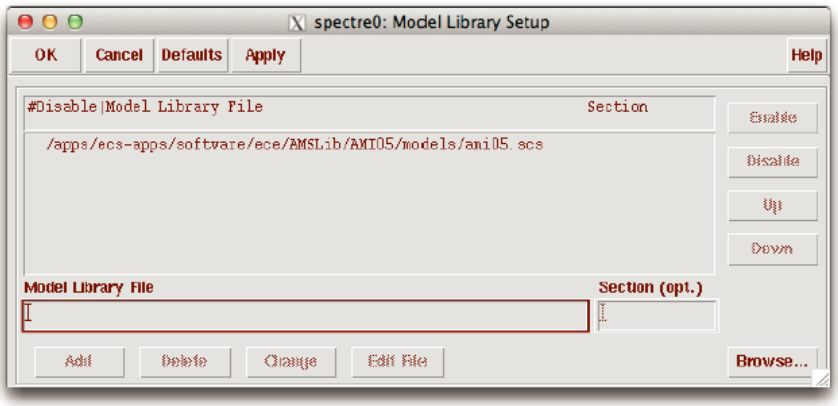


Figure 28: Adding model path.

[STEP 5:] In the Analog Circuit Design Environment window, go to Analysis → Choose. Fill out the form according to Figure 29.

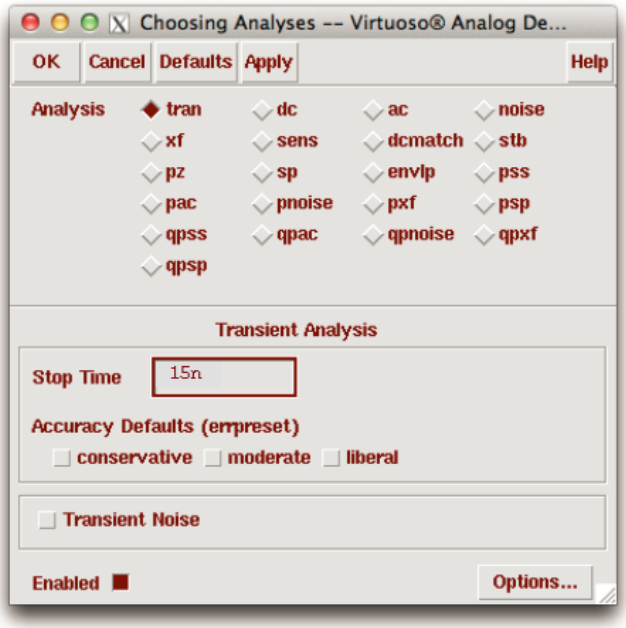


Figure 29: Setting up transient analysis.

[STEP 6:] In the Analog Circuit Design Environment window, go to Outputs → To be Plotted → Select on Schematic. Then go back to the testinv schematic window and select the Vin and Vout wires. Note, the wires should change color after selected, and the signals should be added in the outputs window as in Figure 30.

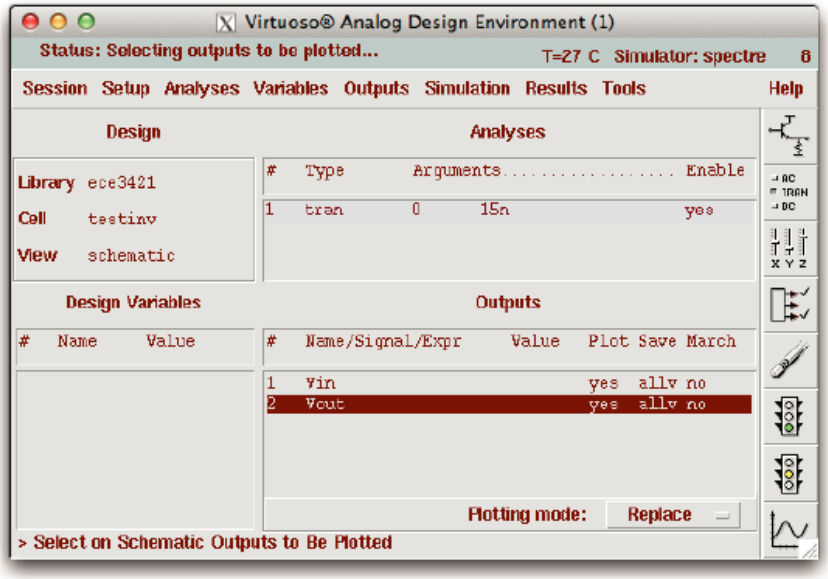


Figure 30: Analog Circuit Design Environment ready for a simulation.

[STEP 7:] In the Analog Circuit Design Environment window, go to Simulation → Netlist and Run. The plot of the simulation should appear in a Waveform Window, like Figure 31.

[STEP 8:] Add a marker to show the switching threshold, save the plots with marker for the report, and finish problem 2.

[STEP 9:] Exit the Analog Circuit Design Environment Simulation window, and then exit the Virtuoso Schematic Editing window.

[STEP 10:] In the CIW window, go to File → Exit. Make a copy of files for future reference, and now you've finished all the contents of Lab-1 of ECE 3421.

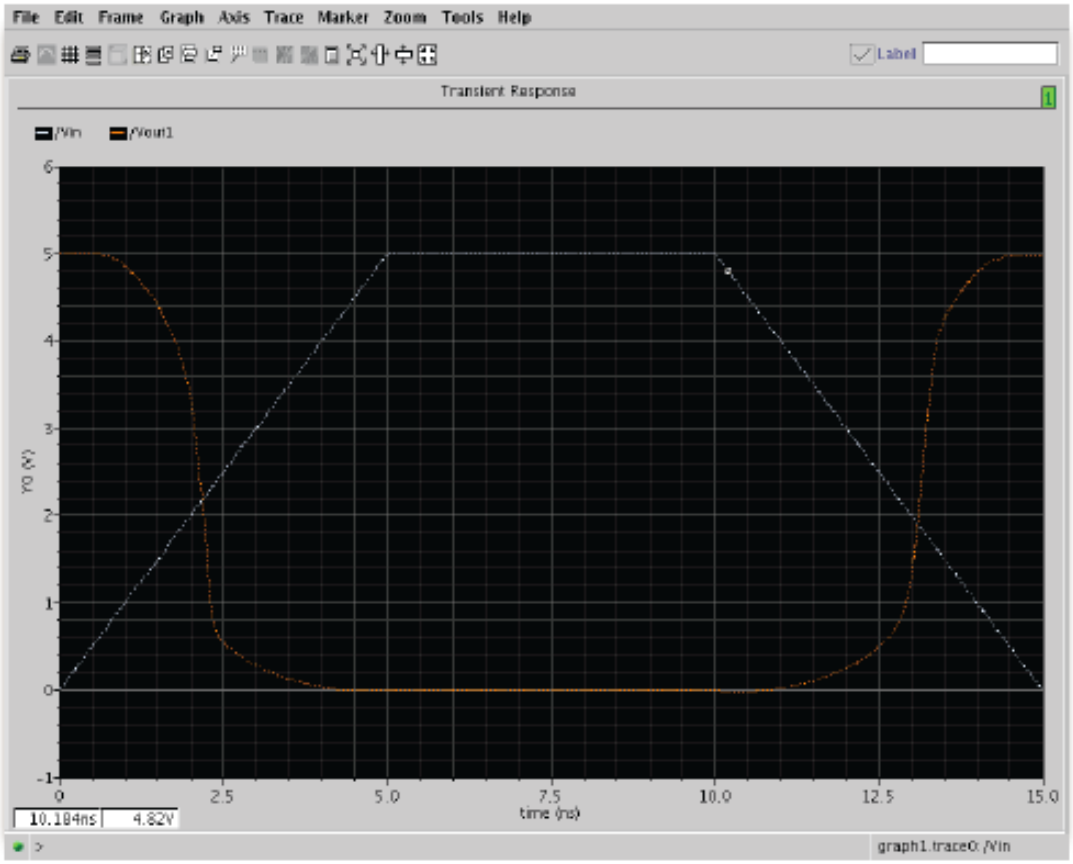


Figure 31: testinv simulation result.

Assignment

1. What values of W or L for the pMOS transistor would change the switching threshold to exactly 2.5V using DC analysis? What does this tell you about the ratio between the k's for the two transistors? Hand in Cadence Vout vs. Vin plots for this configuration.
2. What values of W or L for the pMOS transistor would give a switching threshold of 2.5V using transient analysis? Hand in Cadence Vout and Vin plots for this configuration. (Hint: the transistor sizes in the transient analysis may be different from DC analysis.)