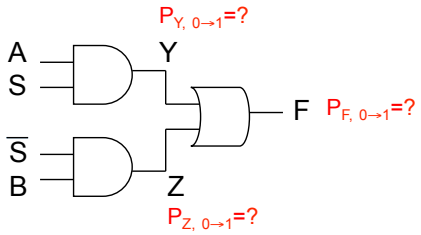
ECE 3421 – VLSI Design and Simulation, Spring 2013

Homework Assignment 4

1. Compute the switching power consumed by the multiplexer shown below assuming that all significant capacitances have been lumped into C=0.3pF. Assume that V_{DD} is 2.5V and the inputs A, S, $\overline{S}$ and B have signal probabilities of 0.5 each with events occurring at a frequency of 100MHz. (Hint: Total switching activity is the sum of the switching activity of individual gates)



2. Design a 4:1 multiplexor (MUX)
(a). Using a combination of transmission gates and logic gates
(b). Using only CMOS logic gates
(c). Which is more efficient in terms of transistors used?

3. Design a pass-transistor network that implements the following function:
Z = A.B.C + A.$\overline{B}$.$\overline{C}$ + $\overline{A}$.$\overline{B}$.C + $\overline{A}$.B.$\overline{C}$

4. Implement the two logic functions F = A+B+C and G = F+D in two stages of cascaded domino logic to minimize transistor count. Show all the required MOS transistors. The design must have at least two stages.

5. Draw the schematic and layout of F = $\overline{A.(C+D)+B}$. (Hint: You may determine the order of A, B, C, and D inputs using the Euler path method).